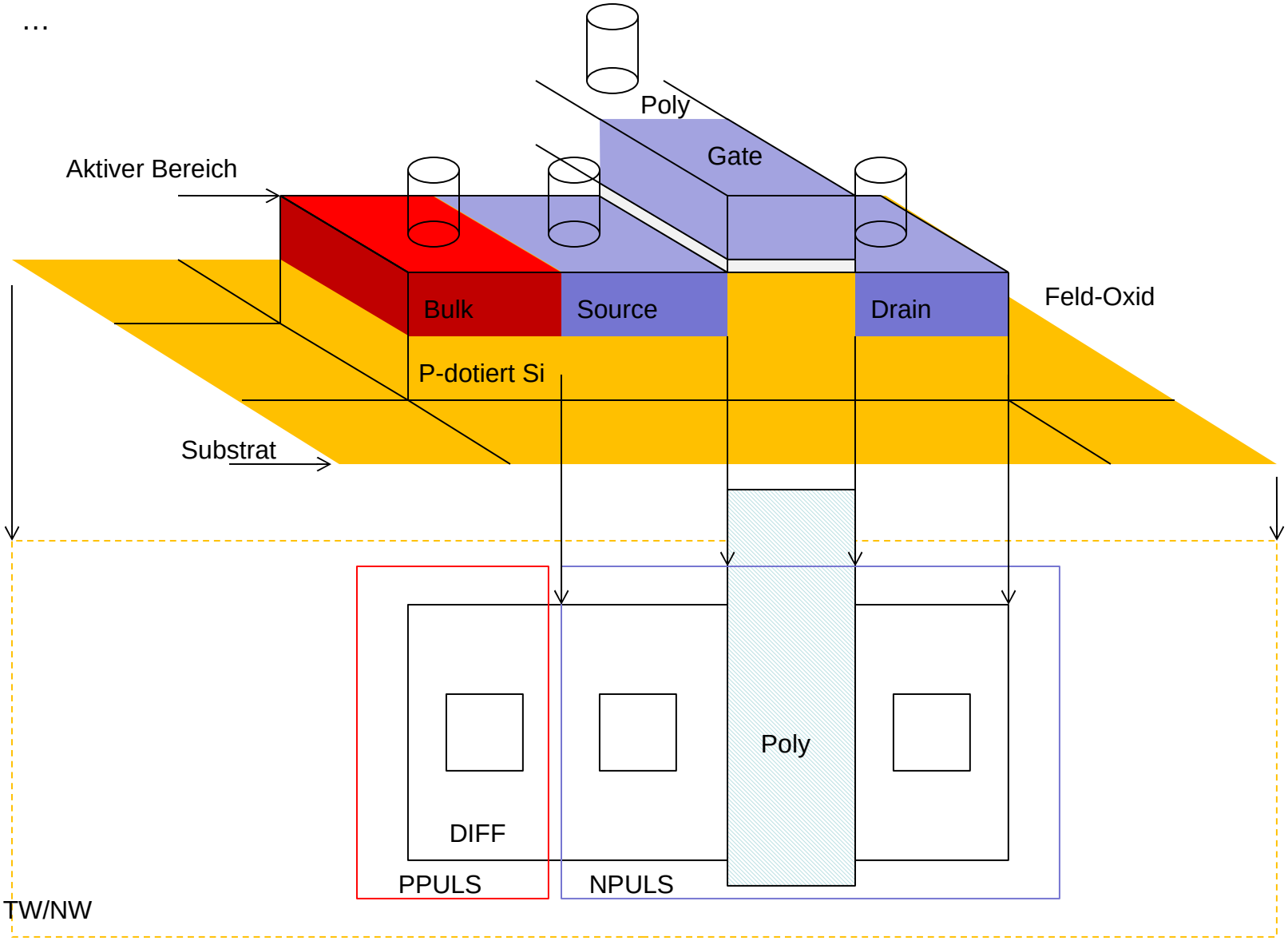
Layout

Layout

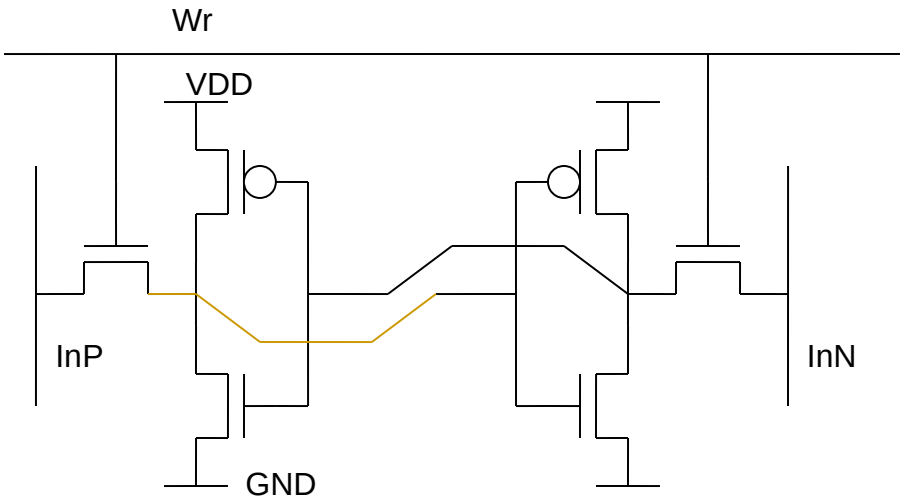
Layout

- …


Poly
Gate
Aktiver Bereich
Bulk
Source
Drain
Feld-Oxid
P-dotiert Si
Substrat
Poly
DIFF
PPULS
NPULS
TW/NW

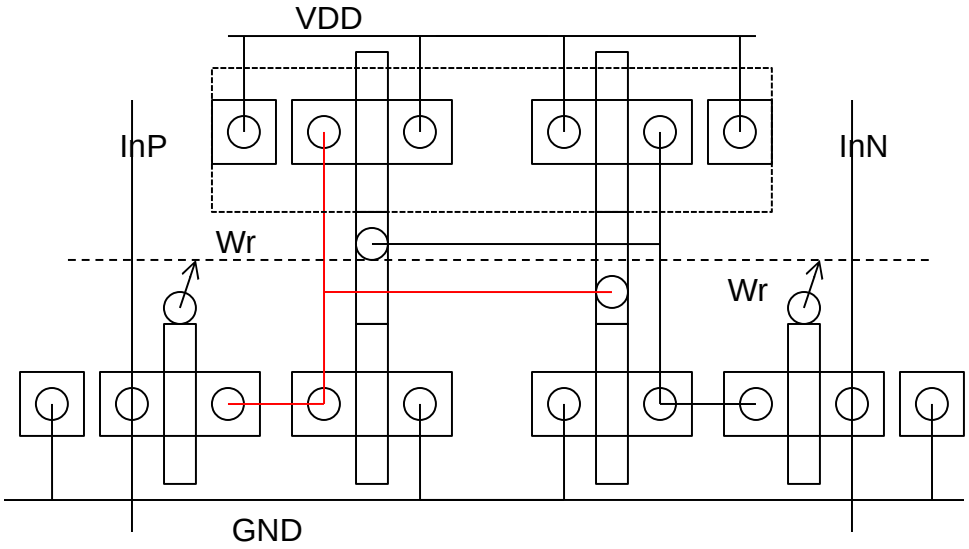
Layout

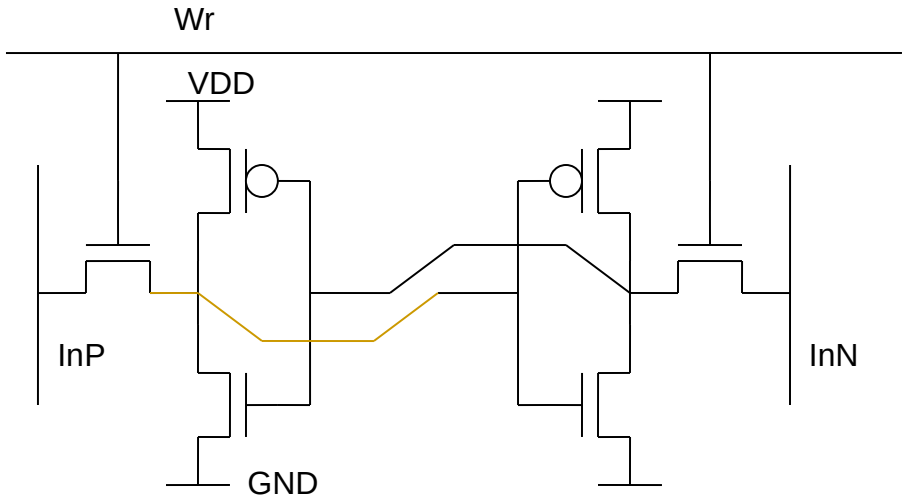
- …



Layout

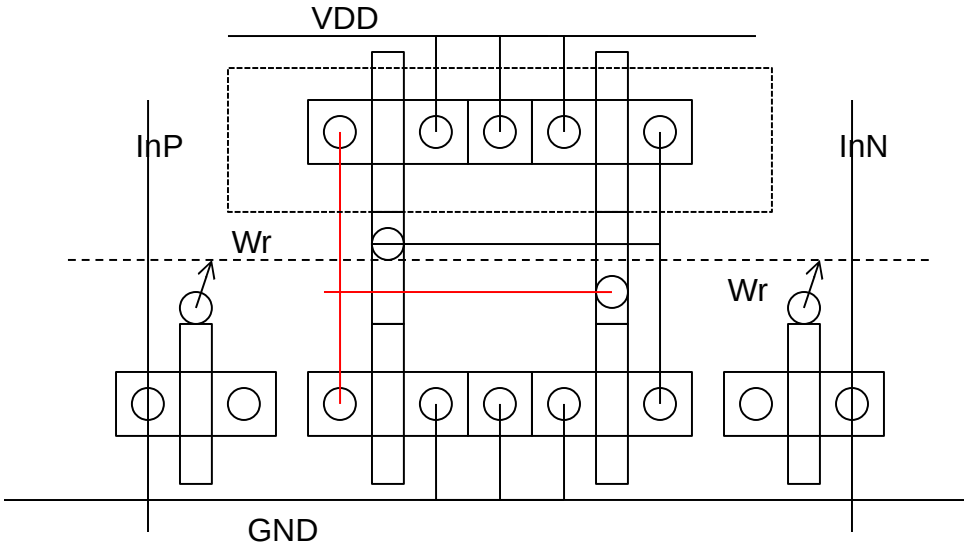
- …

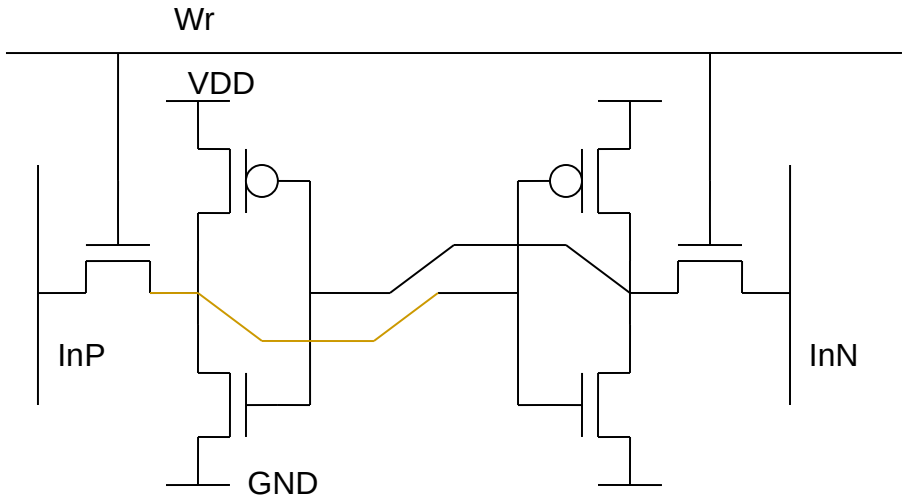




Layout

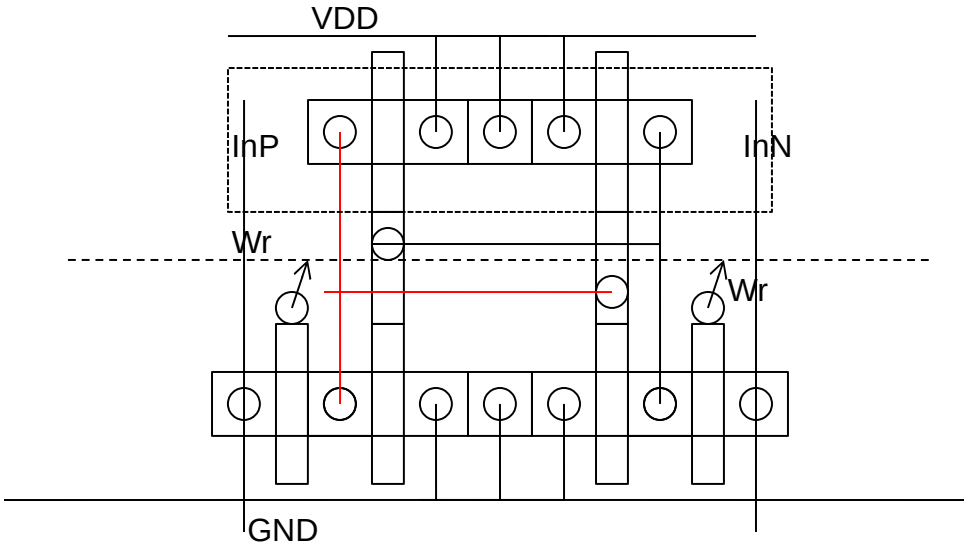
- …

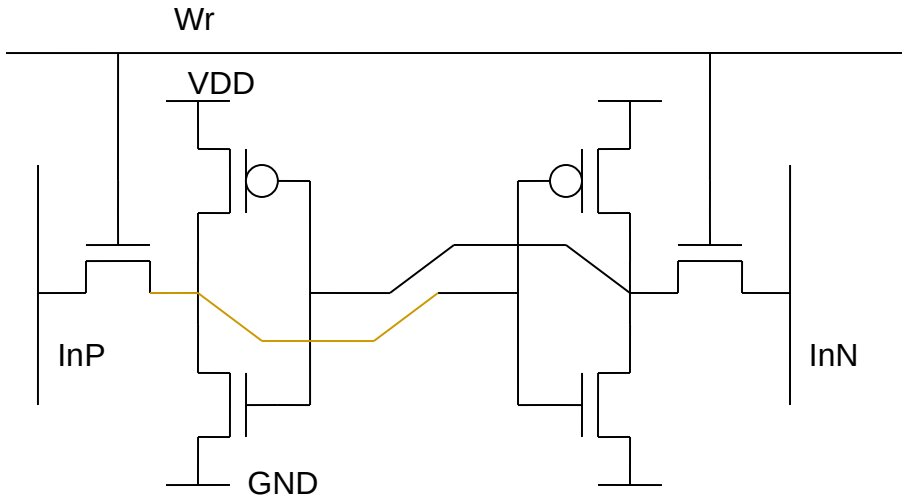




Layout

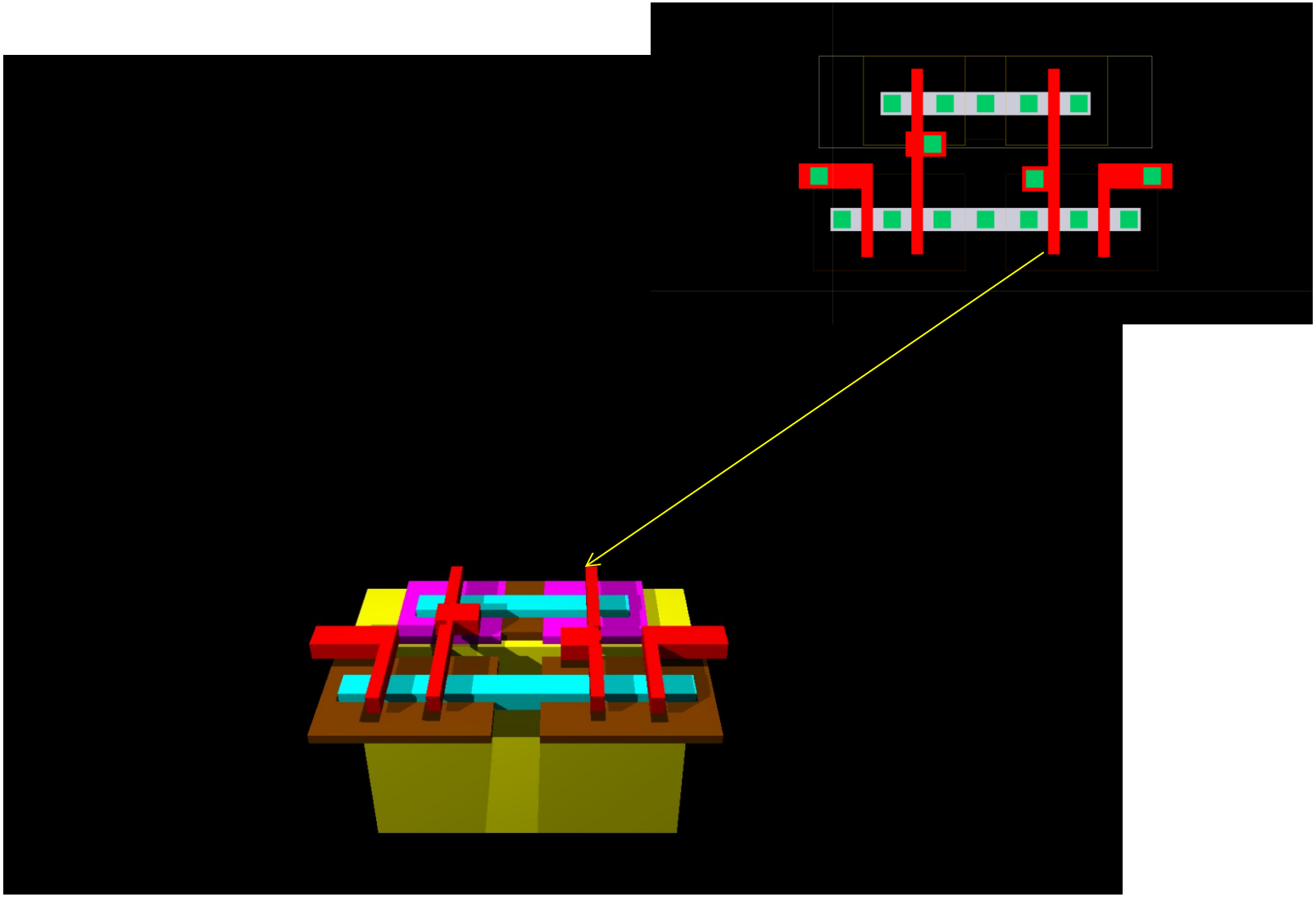
- …





Layout

- …



Layout

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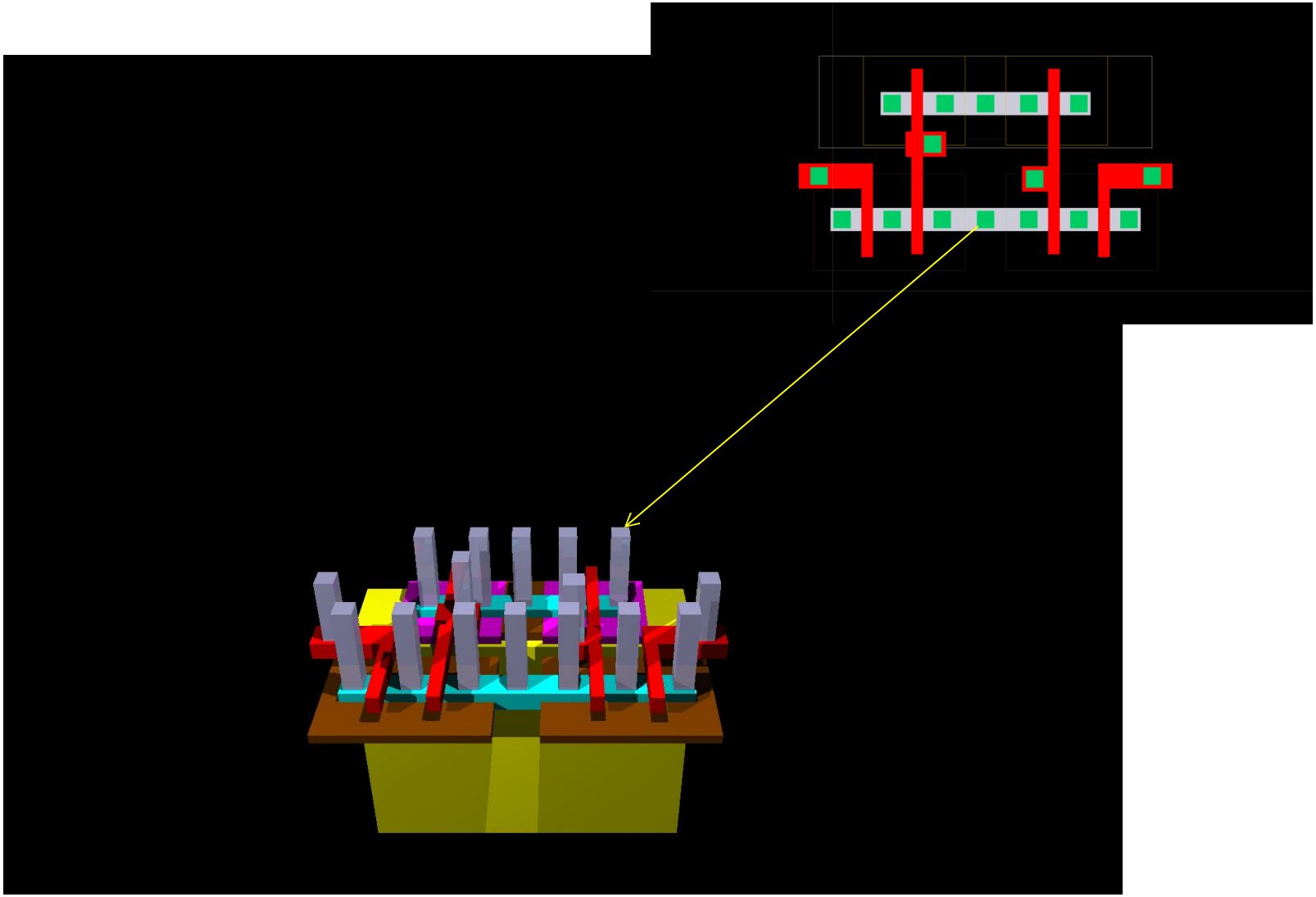
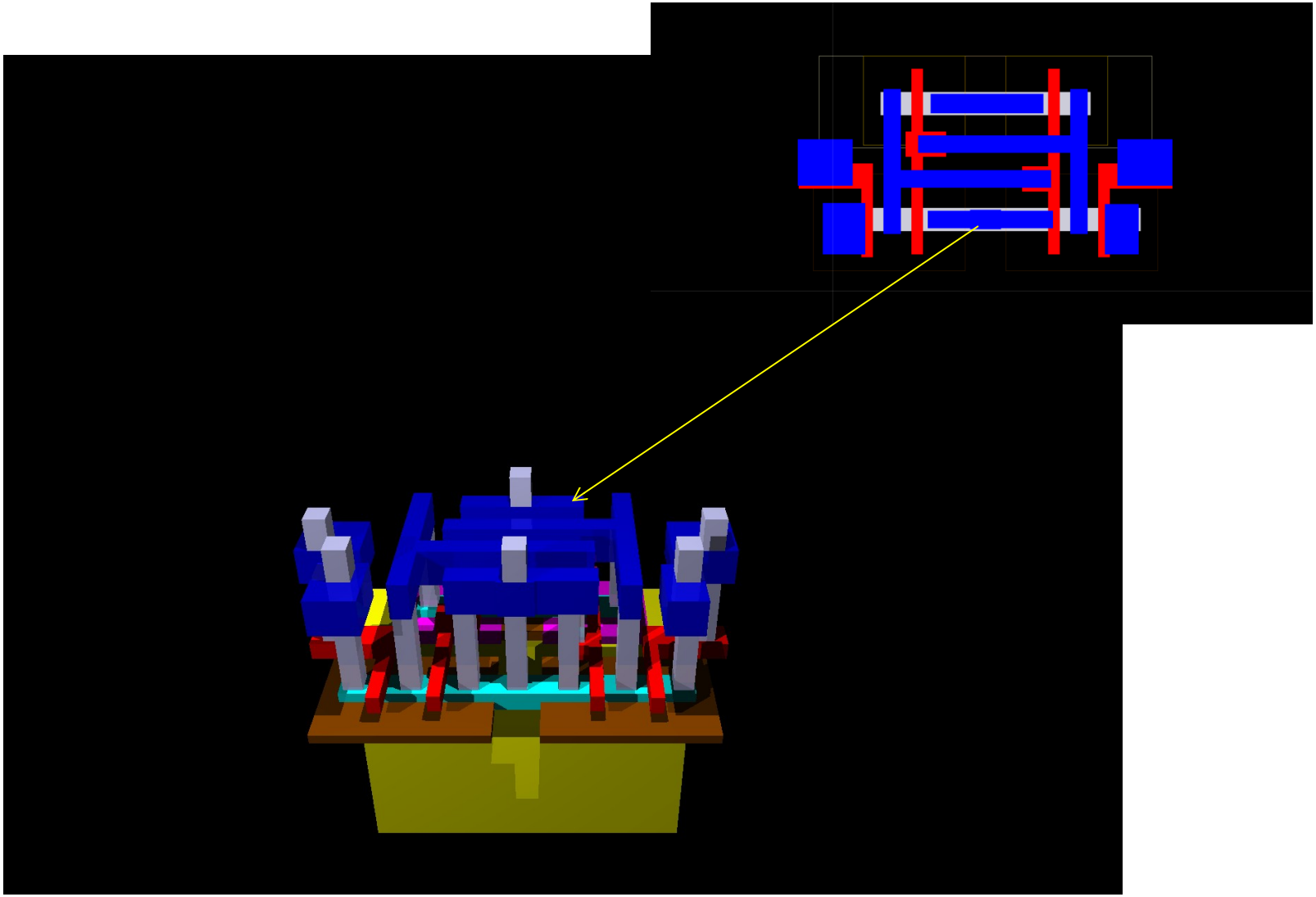


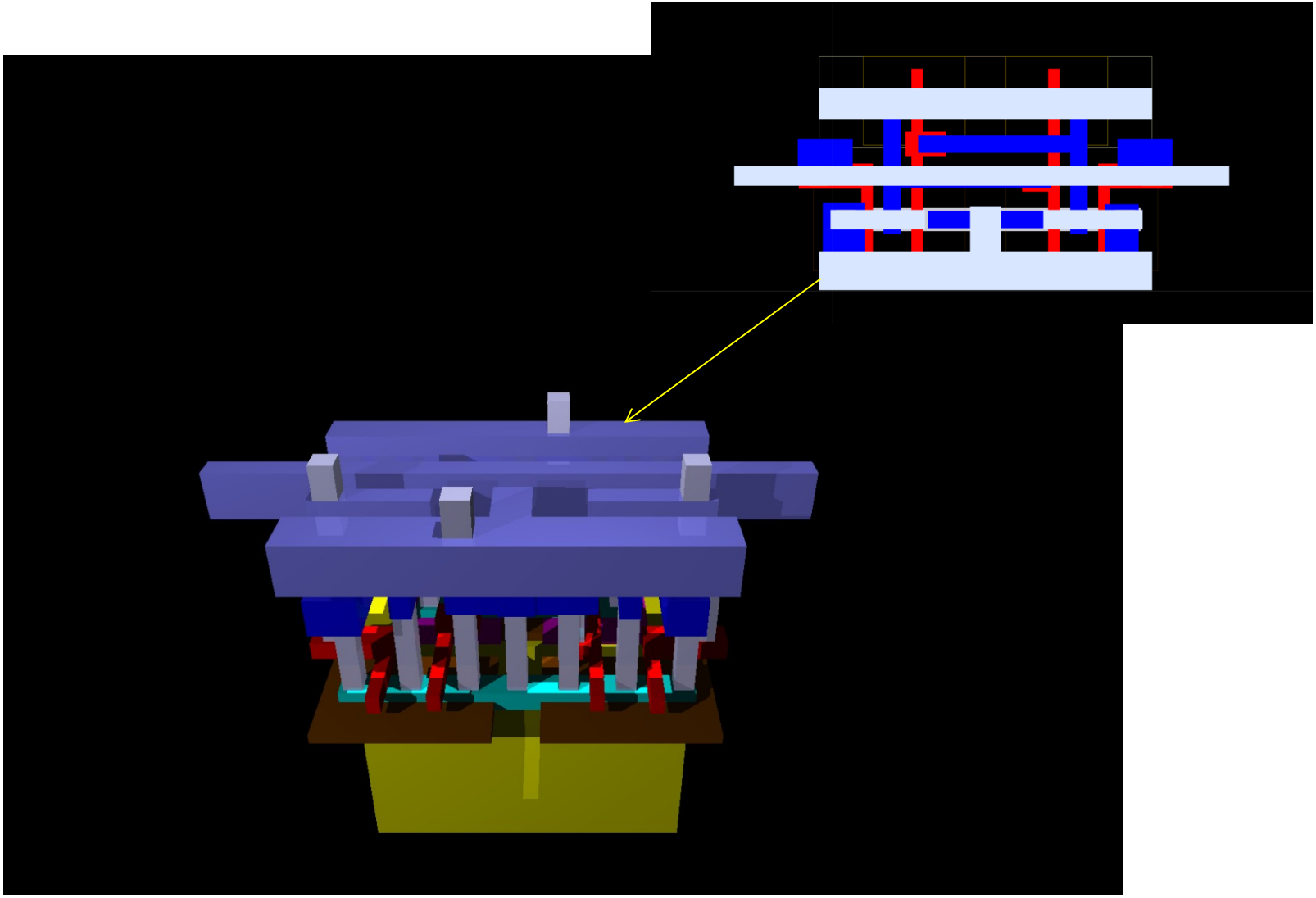
Layout

- …



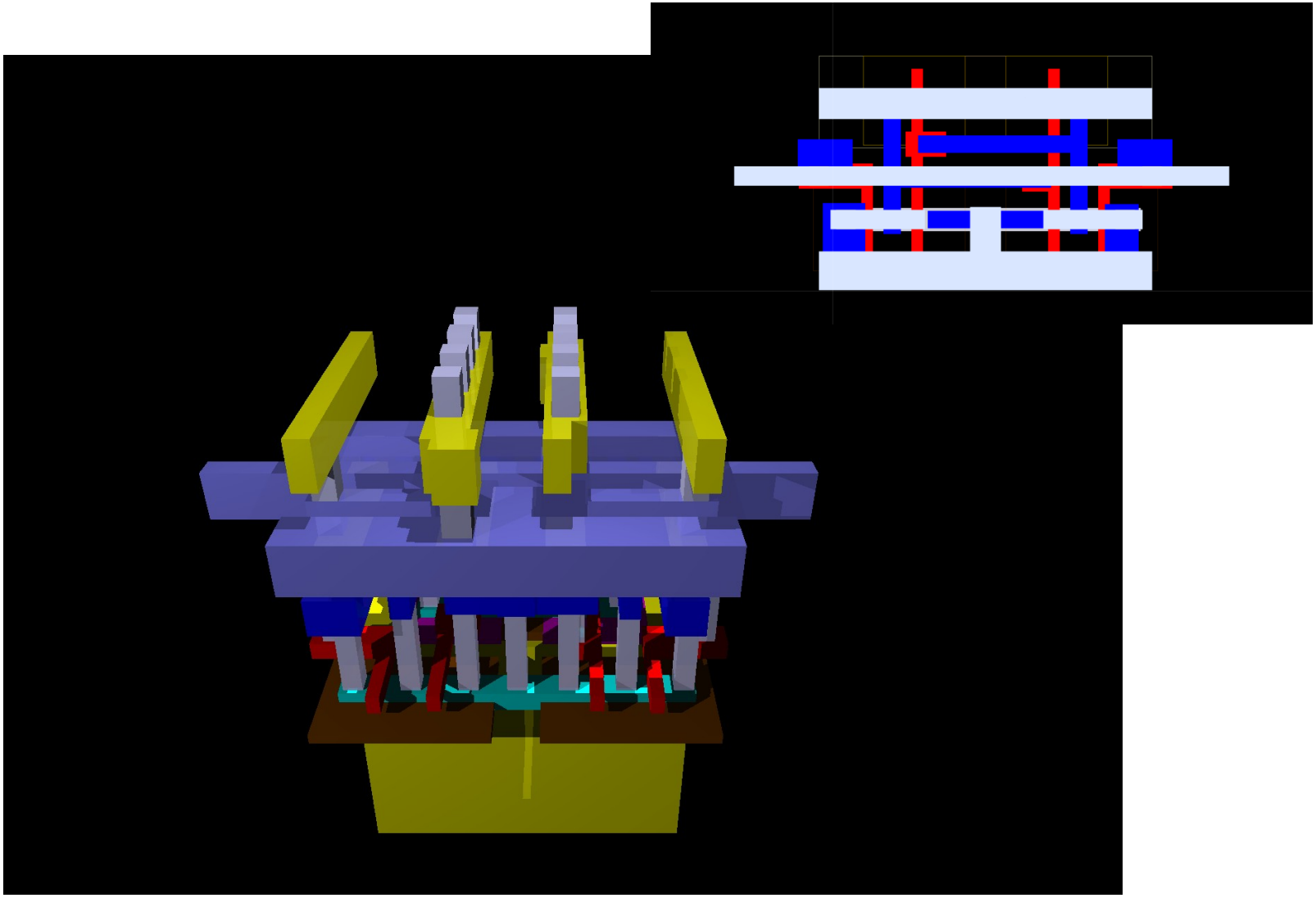
Layout

- …



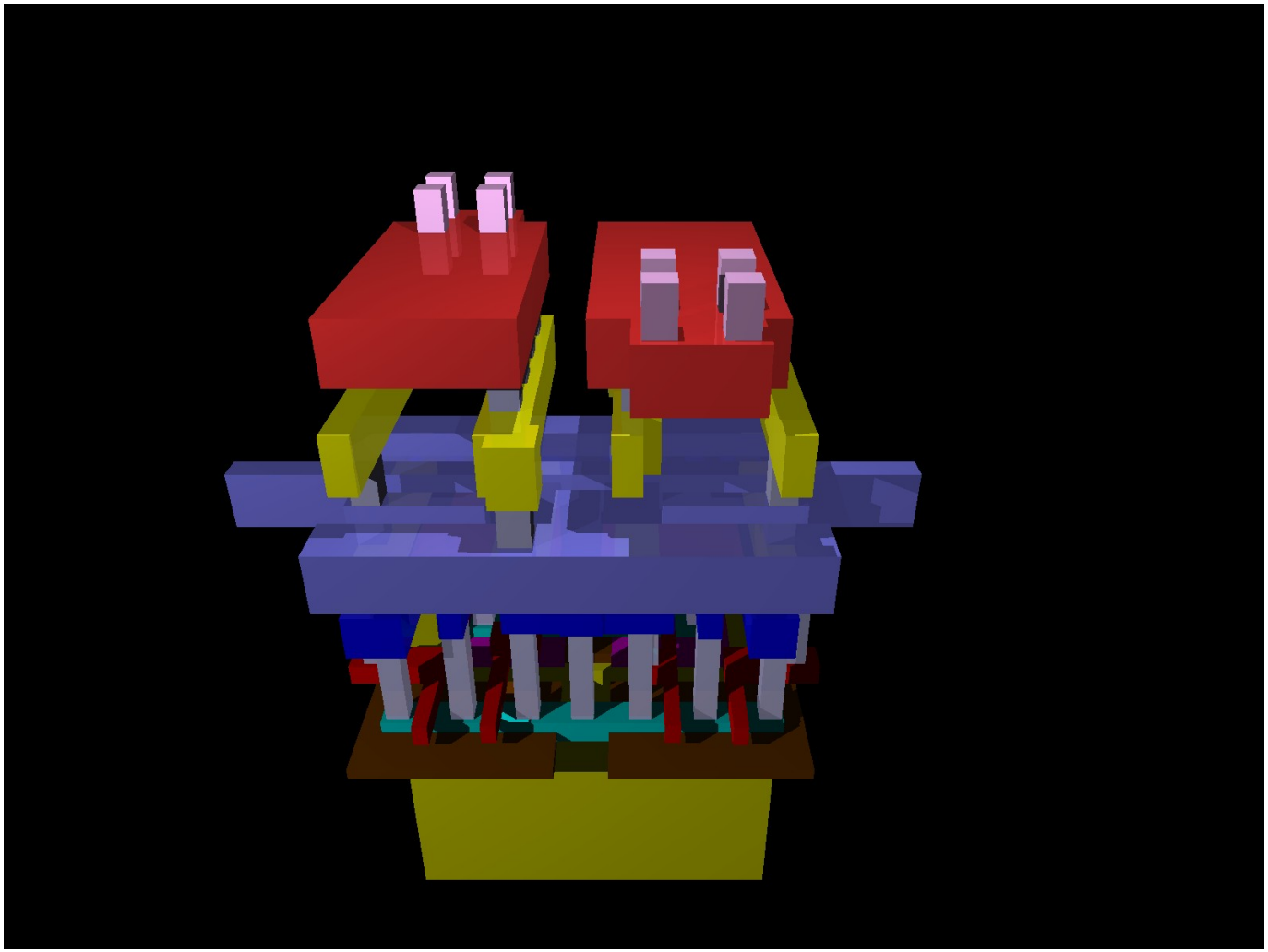
Layout

- …



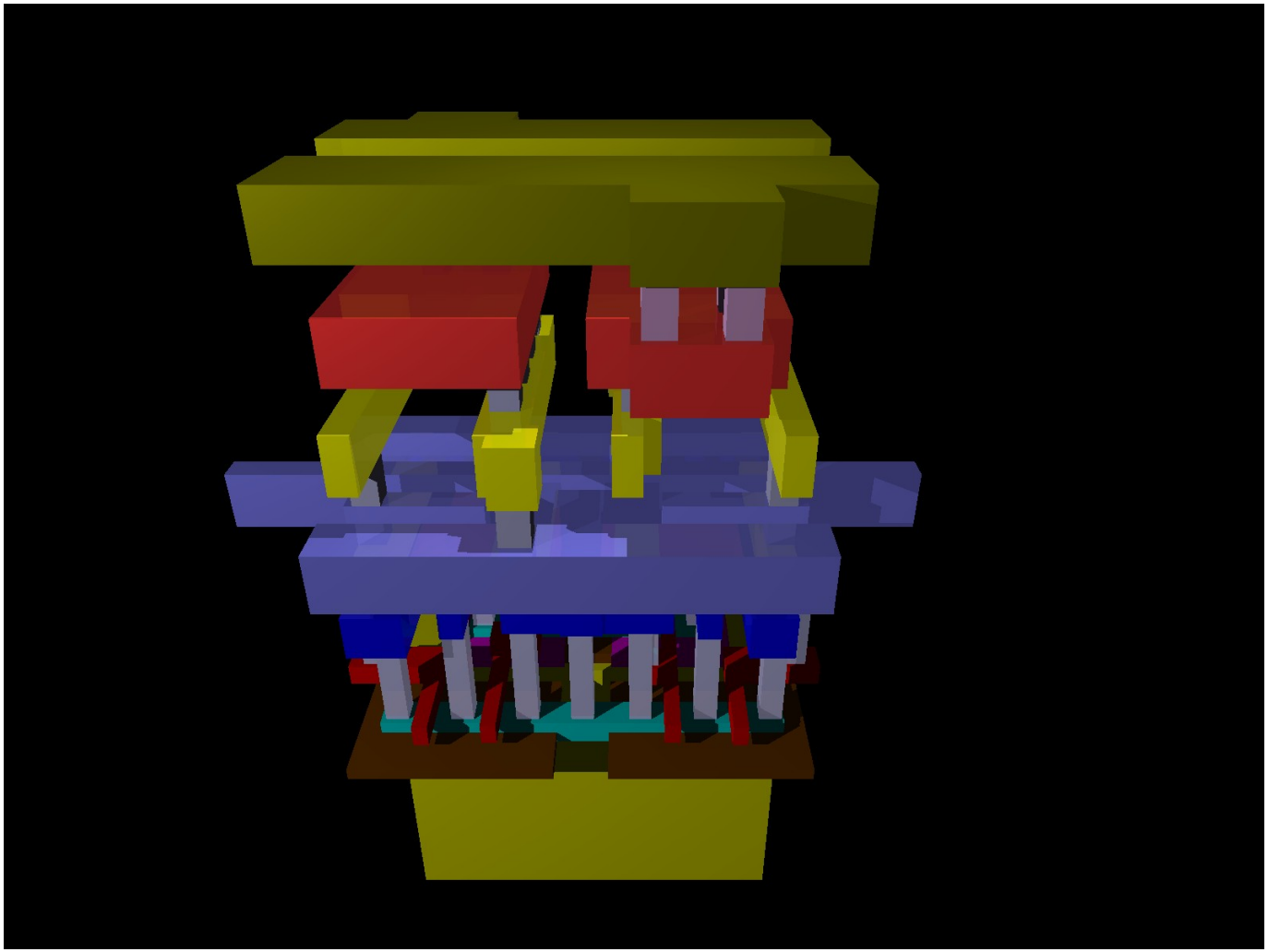
Layout

- …



Layout

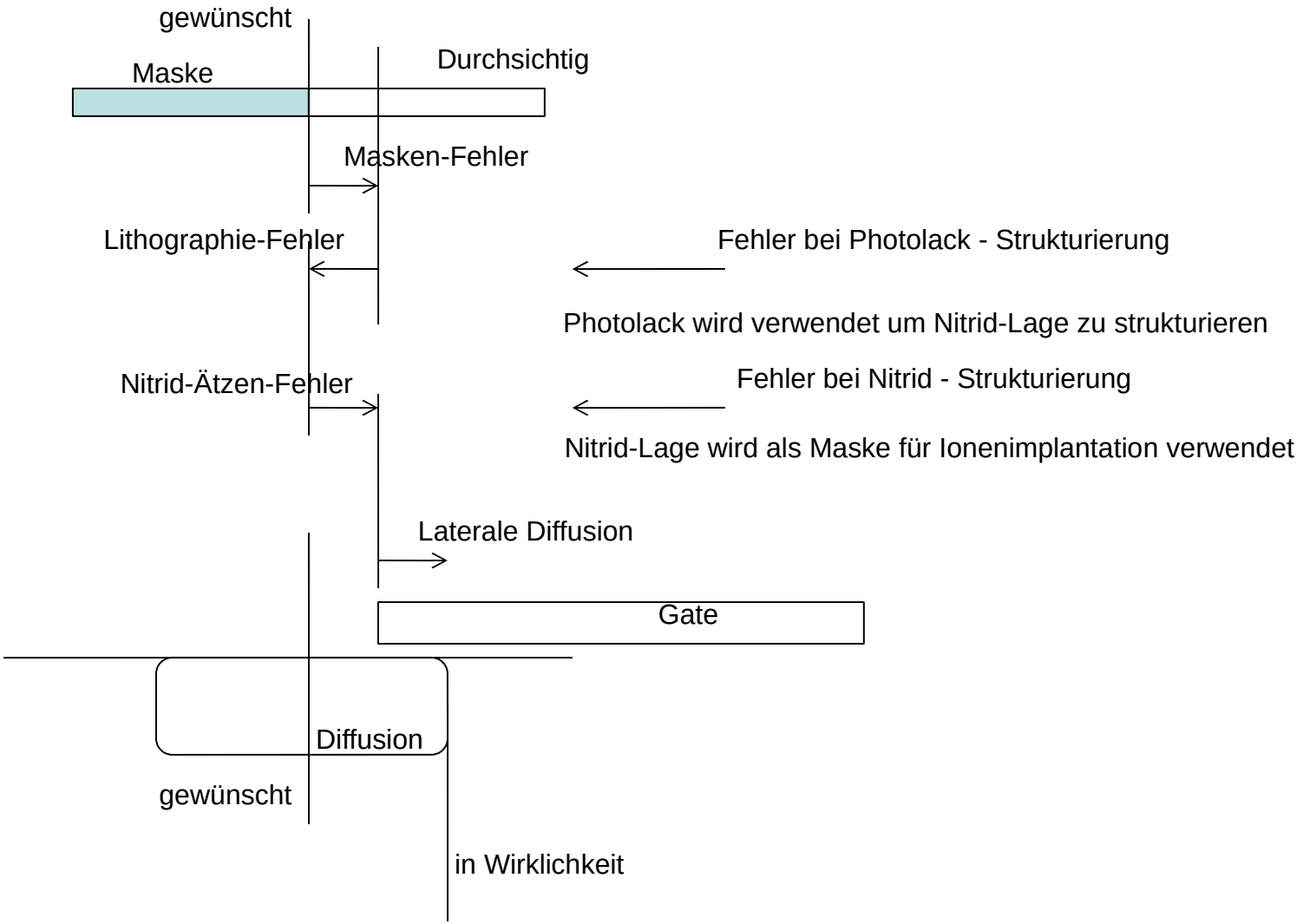
- …



Designregeln

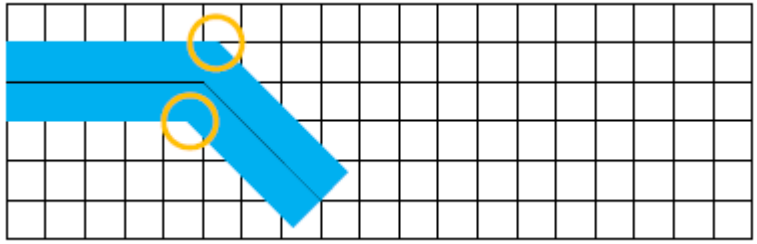
Layoutregeln

…



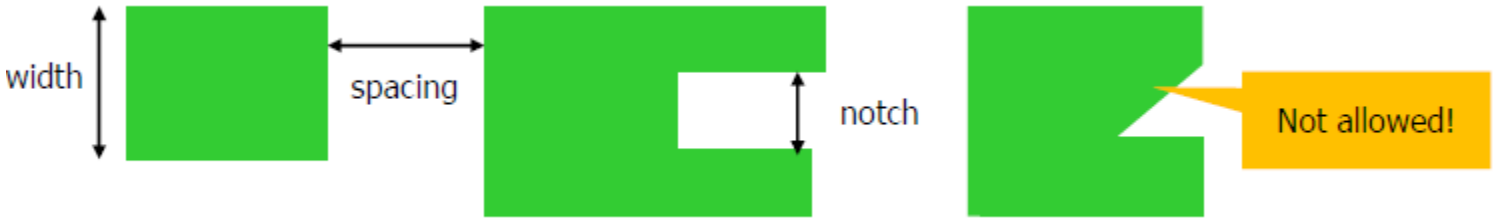
Layoutregeln

- Grid Regeln
- Alle Ecken müssen auf einem Raster liegen
- *Problem wenn bei einem 45° „Path“*

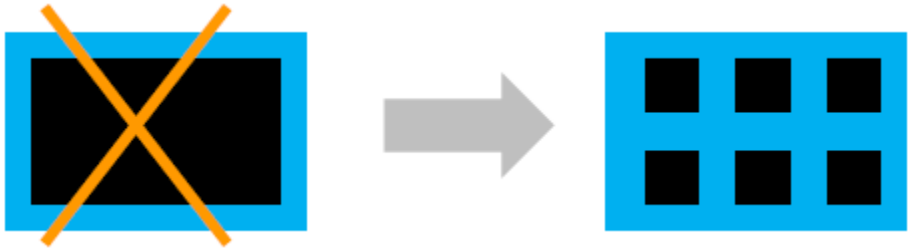


Layoutregeln

- Minimale Geometrieregeln

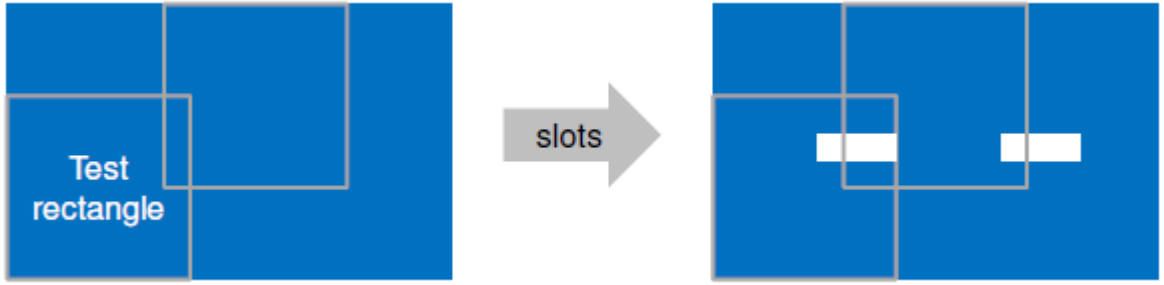


- Manche Strukturen (Kontakte – Vias) haben eine feste Größe
- Wenn eine größere Fläche benötigt wird, zeichnet man eine Matrix



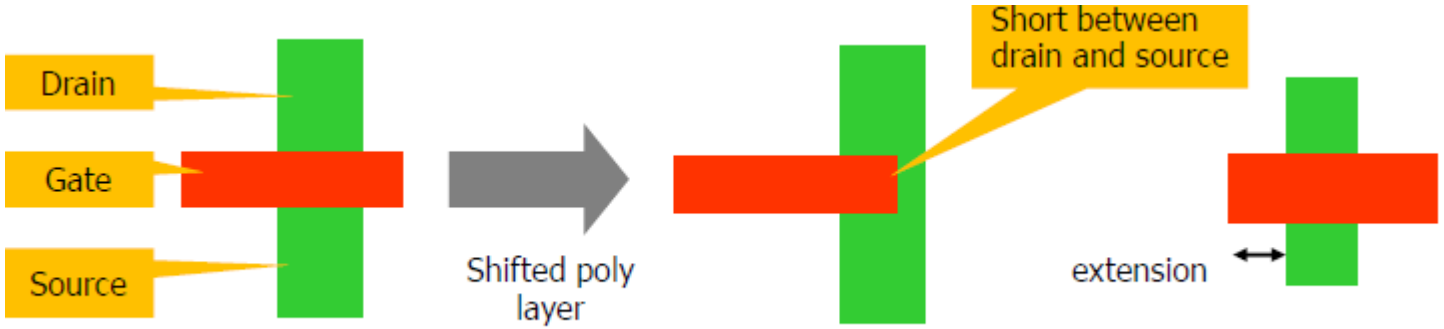
Layoutregeln

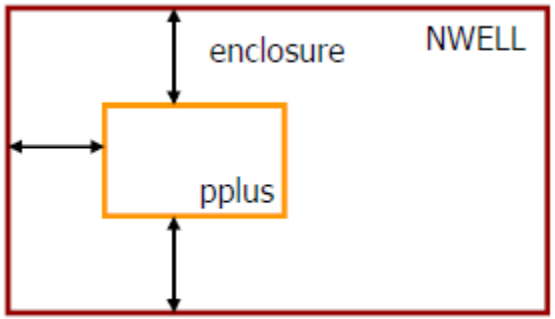
- Es gibt auch Maximum-Regel
- Strukturen dürfen nicht zu groß sein
- Beispiel – wenn Metallleitungen zu breit sind, werden Schlitze gezeichnet – dafür gibt es eine spezielle Lage



Layoutregeln

- Regeln zwischen verschiedenen Lagen
- Extension-Rules

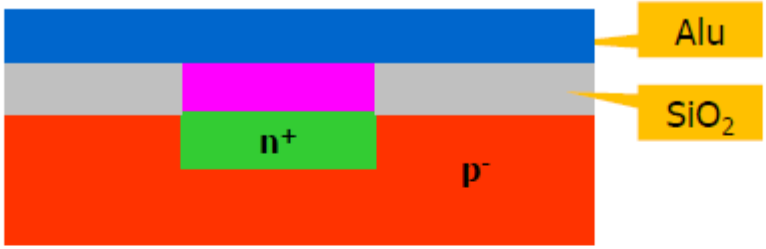




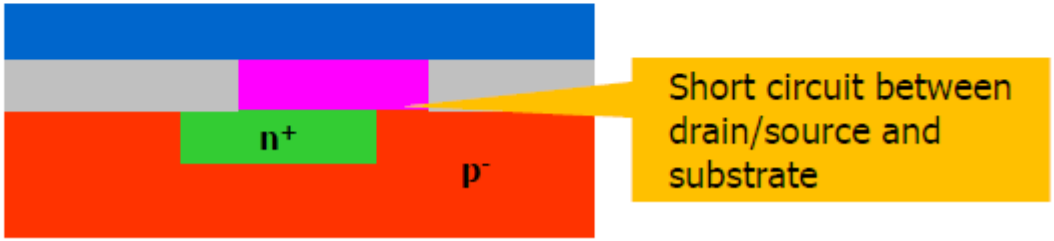
Layoutregeln

- Überlapp-Regeln
- Kontakte

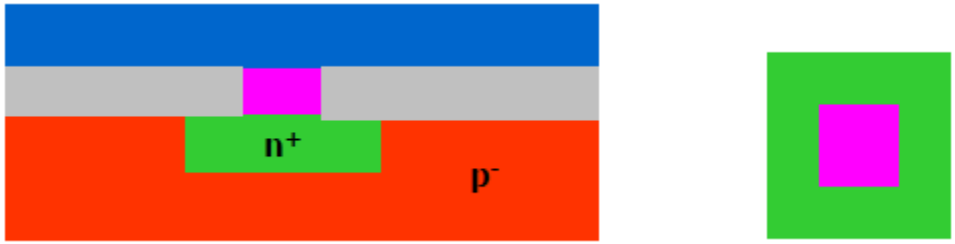
Ideal
(minimal n^+ size)



Misaligned
contact mask:

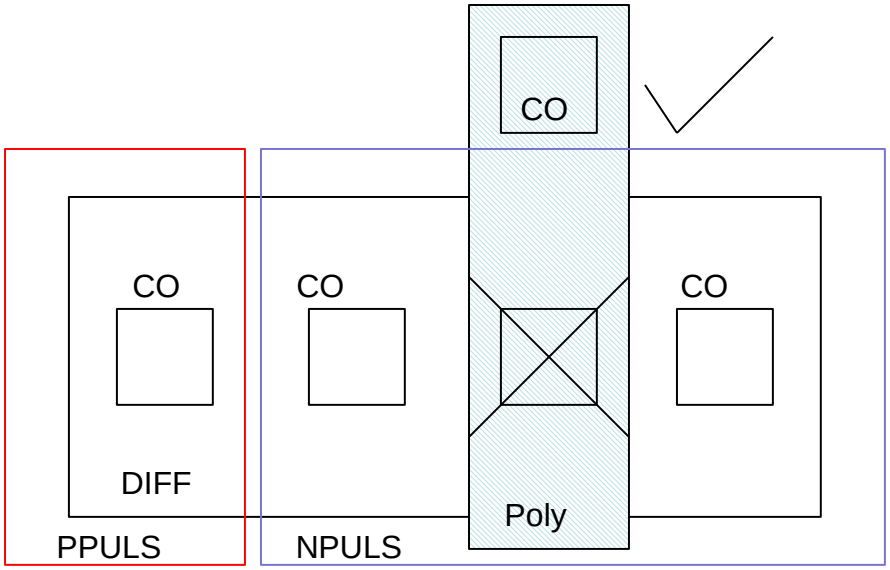


- Richtig – Kontakt kleiner als n+ aktive Lage

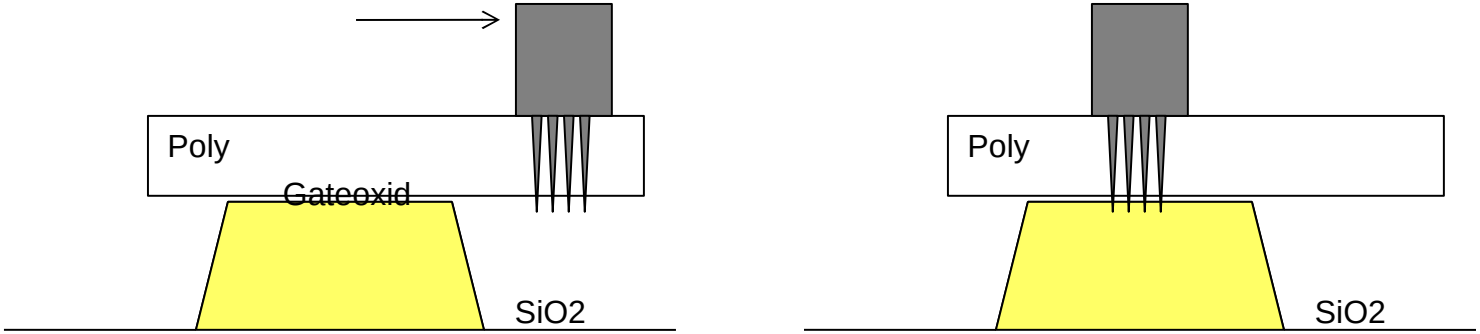


Layoutregeln

- CONTACT: Verbindung zwischen M1 und Poly, n+, p+
- Kontakt ist über Gateoxid nicht erlaubt

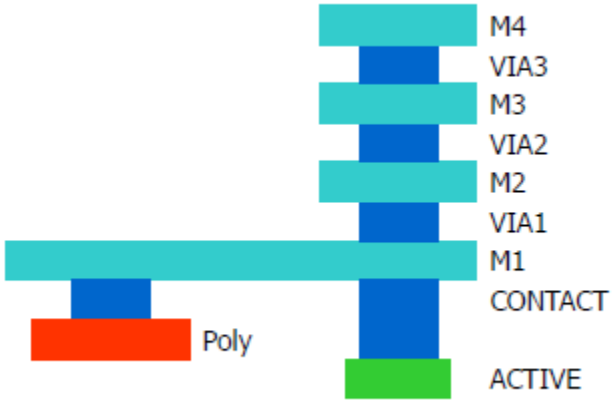


Metalle diffundieren in angrenzende Materialien bei hoher T

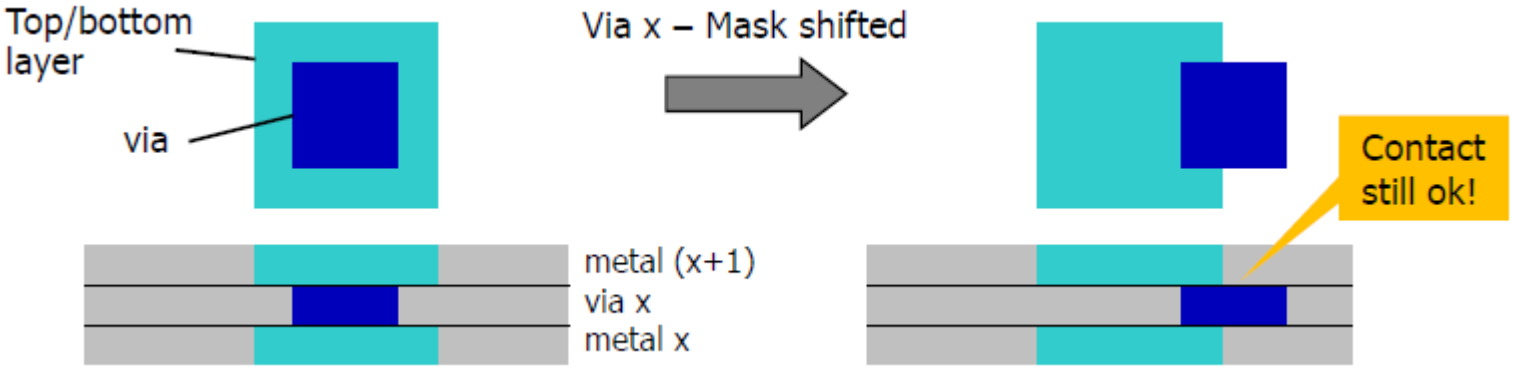


Layoutregeln

- CONTACT: Verbindung zwischen M1 und Poly, n+, p+
- Via i: Verbindung zwischen Metall i und Metall i+1

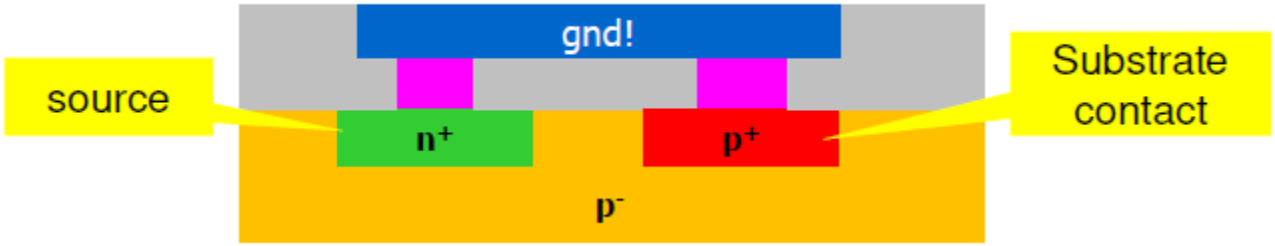


- Via-Maske kann verschoben werden ohne Kuzschluß zu machen

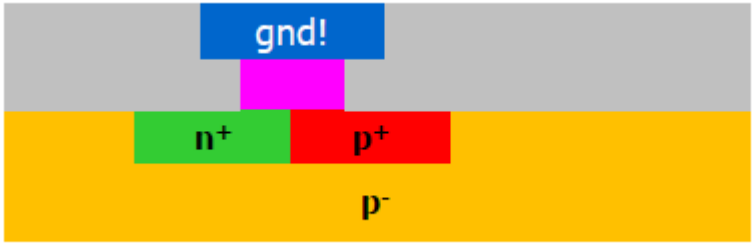


- Enclosure Regeln sind oft nicht so streng:

- Normaler Substratkontakt

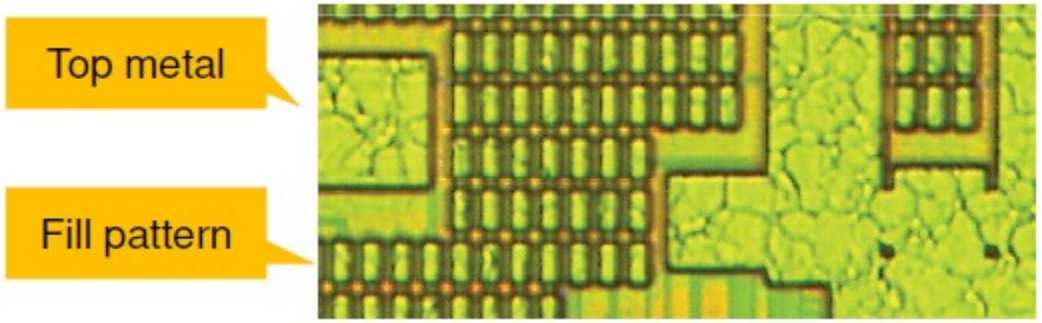


- „Butted“ Substratkontakt



Layoutregeln

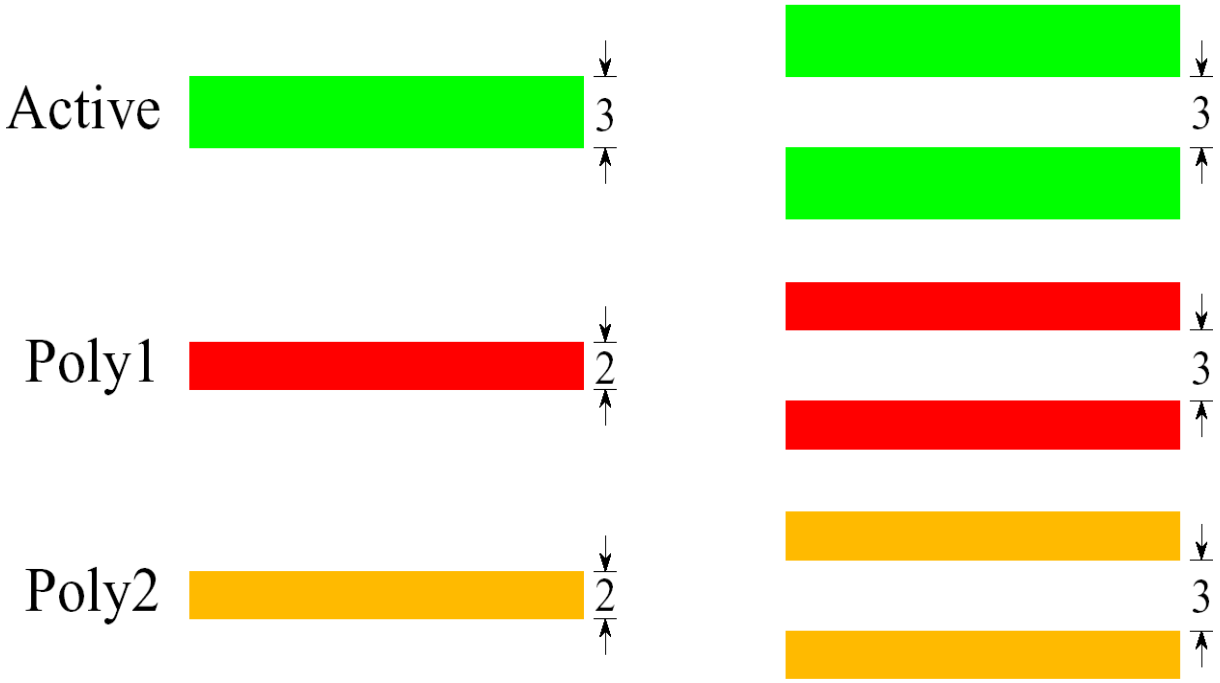
- Füllfaktor sollte auf jeder Lage in einem bestimmten Bereich liegen
- Falls es zu wenige Strikturen gibt werden Füllobjekte hinzugefügt



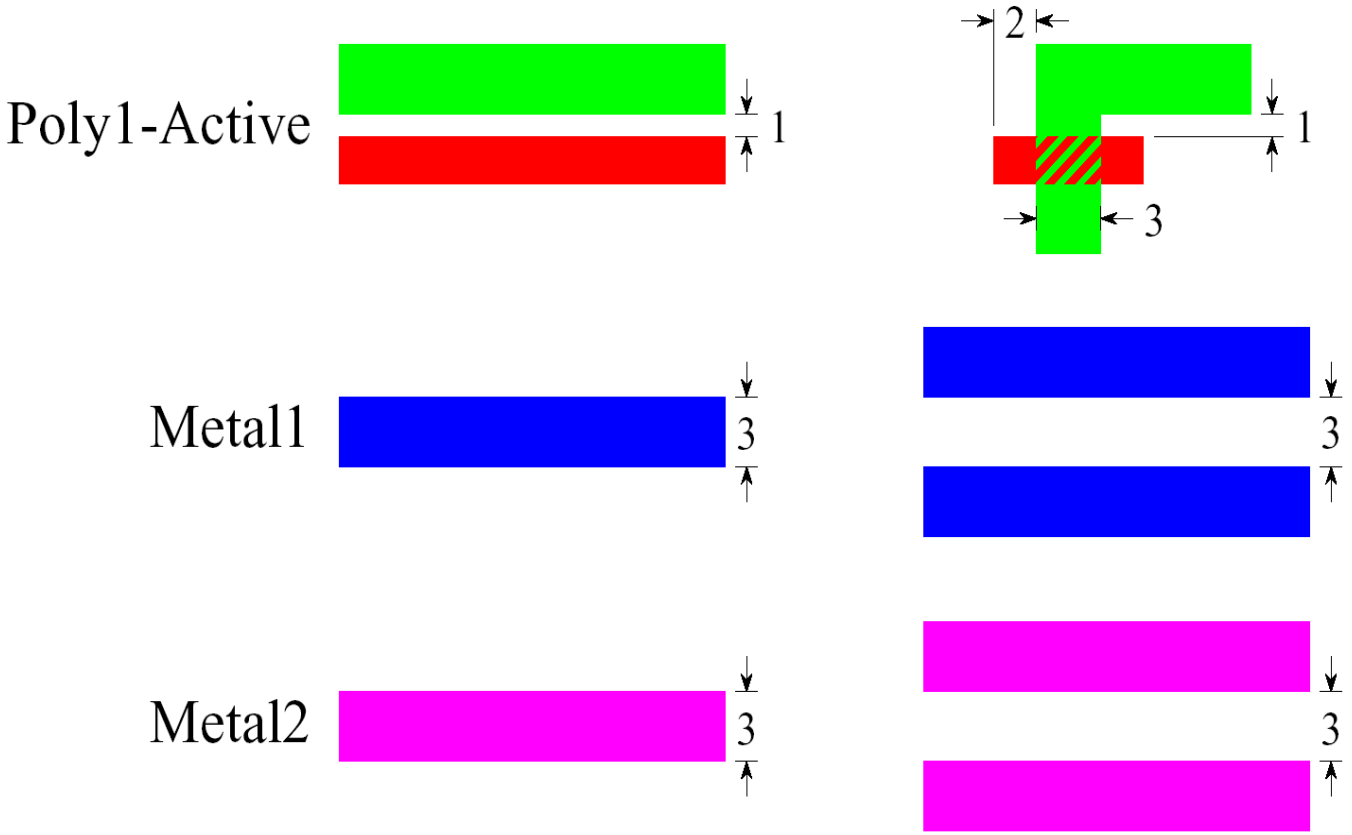
Skalierbarer CMOS-Entwurf

Skalierbarer CMOS-Entwurf

Alle Abmessungen der Struktur der Bauelemente werden in ganzzahligen Vielfachen eines Faktors (z.B. ¬) entworfen.
Die Entwurfsregeln geben an, welche Mindestabmessungen bzw. Mindestabstände die einzelnen Strukturen innerhalb einer Ebene und gegenüber anderen Ebenen eingehalten werden müssen.

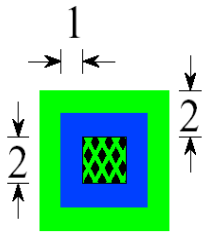


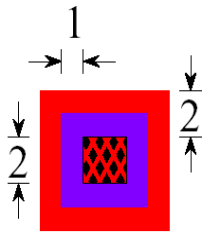
Minimale Breiten und Abstände der einzelnen Strukturen



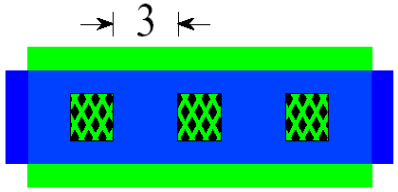
Kontaktbereiche, um die Anschlüsse des Bauelements (z.B. S,D,G) mit Leitungen zu verbinden.
(Löcher im isolierenden Oxid)

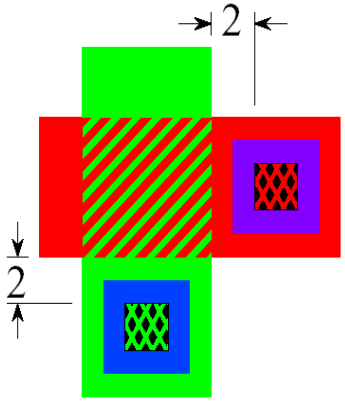
Contacts





Contact Spacing

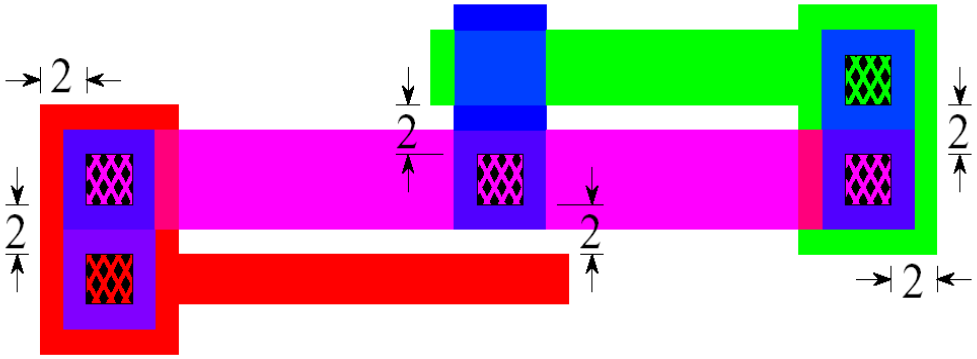




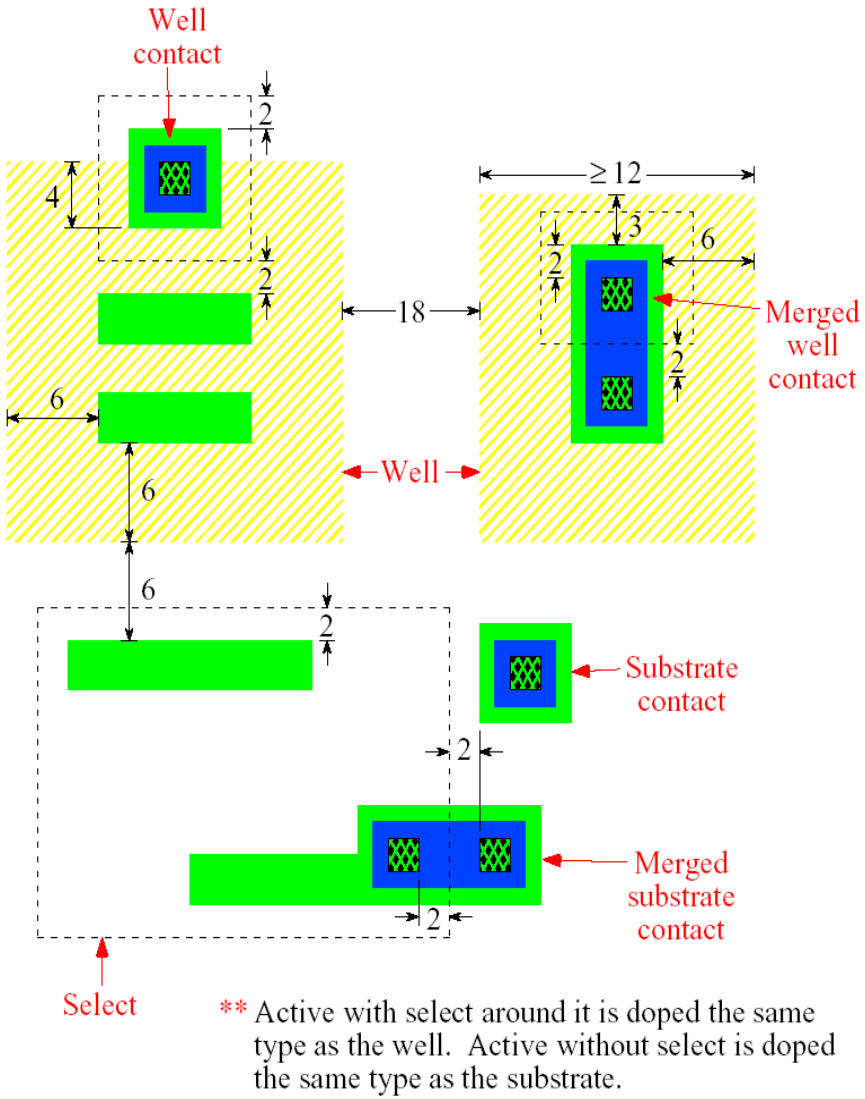
Durchkontaktierung, um von einer Verbindungsebene zur nächsten zu gelangen.
(Löcher im isolierenden Oxid)

Vias

Via Spacing



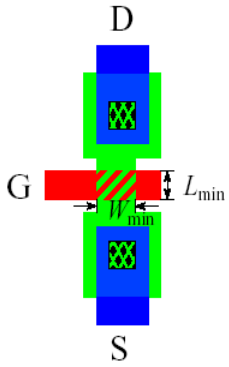
Layoutregeln



Jede Technologie hat ihre eigenen Definitionen. Nicht alle gezeichneten Ebenen haben auch einen Prozessschritt zur Folge.

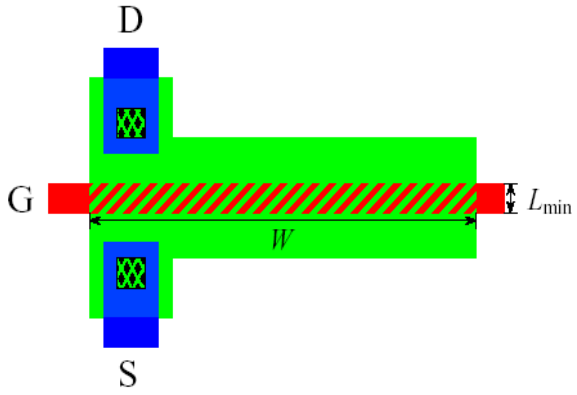
Bauteile

Feldeffekttransistoren (Grundaufbau)

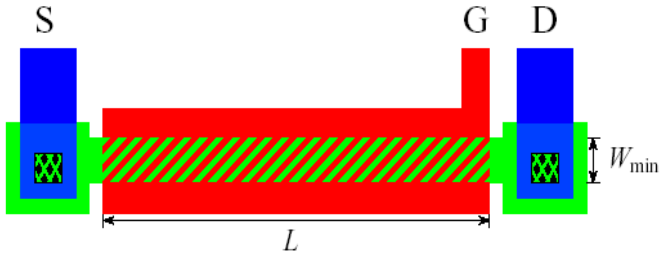


Minimum size

W_{min} and L_{min} set by design rules



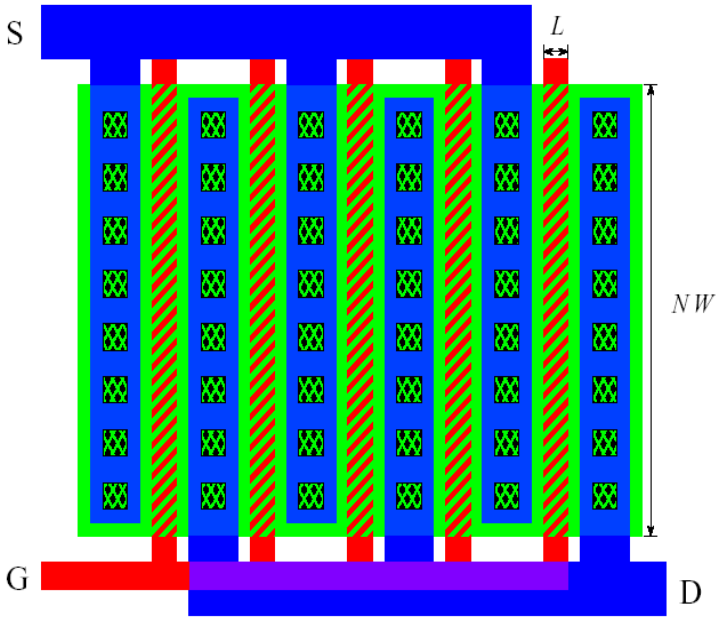
Wide
Strong
Large W/L

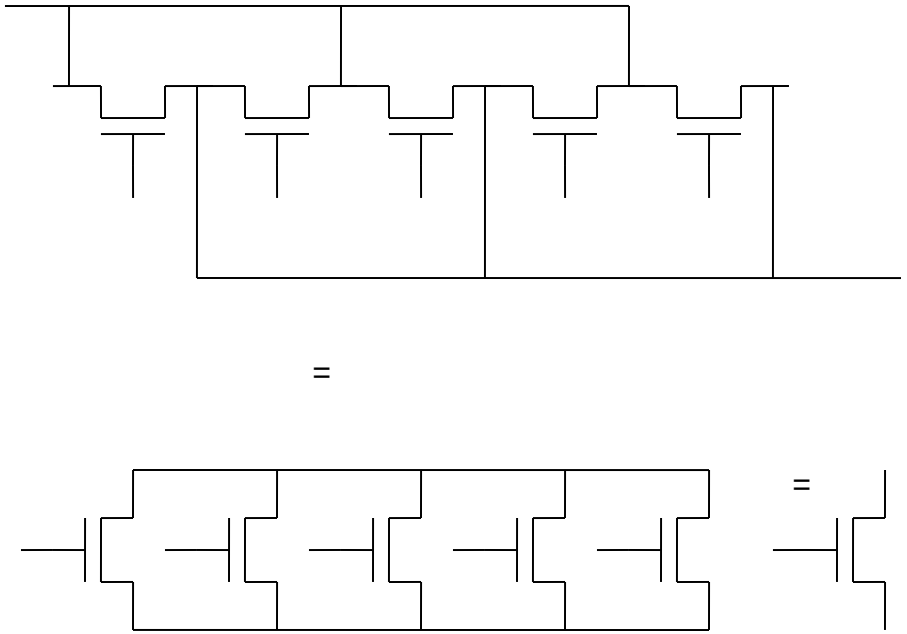


Long
Weak
Small W/L

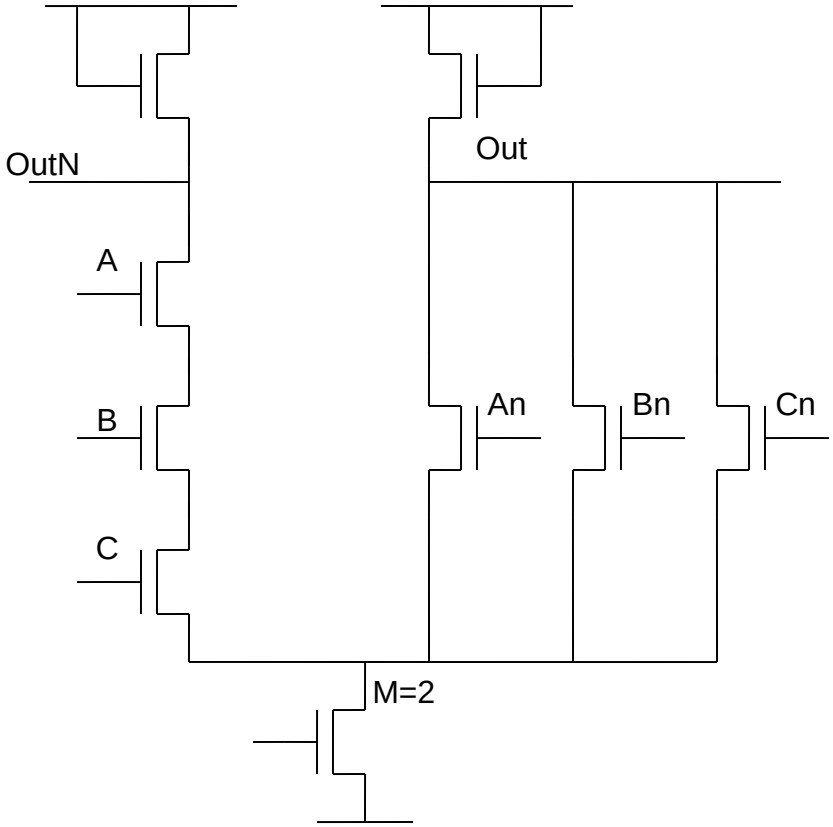
Bauteile - FET

Stacked Transistors:
Durch diesen Aufbau werden in den mittleren Bereiche S + D doppelt verwendet,
d.h. geringere GS- und DS- Kapazitäten



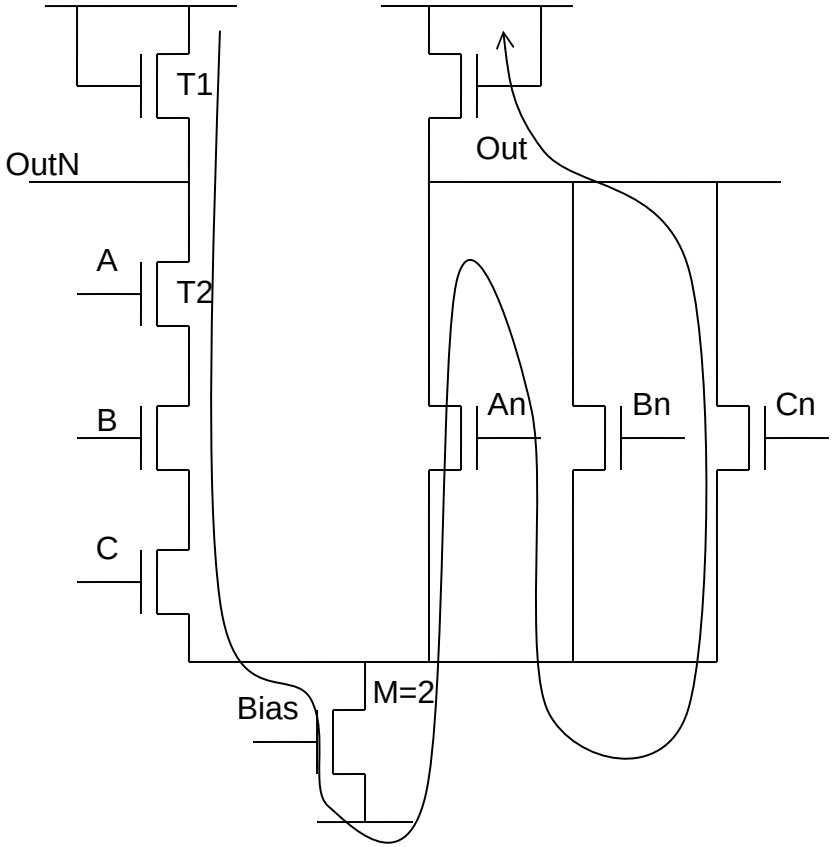


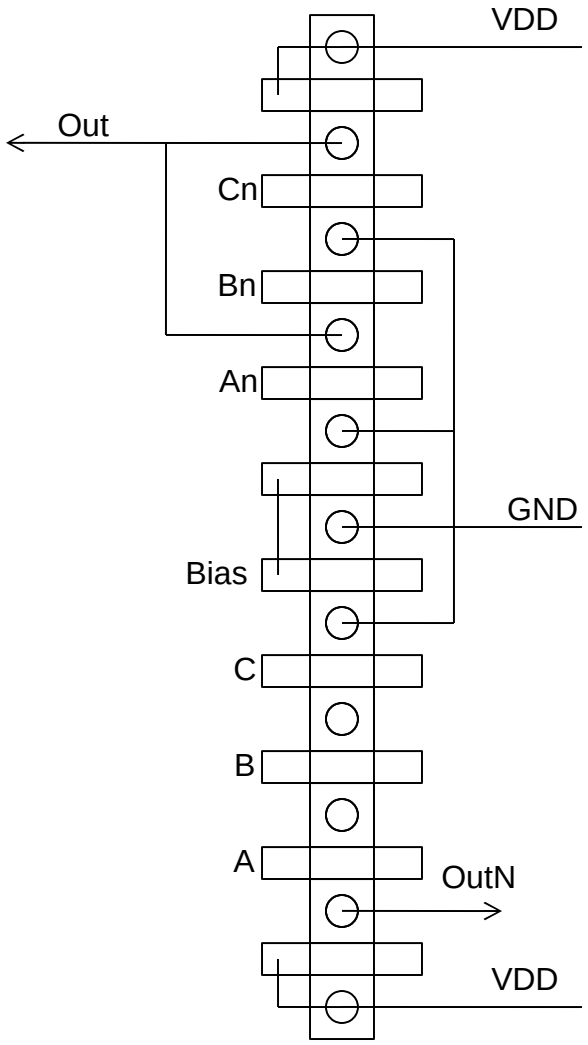
Transistoren in Reihe



Out = A and B and C

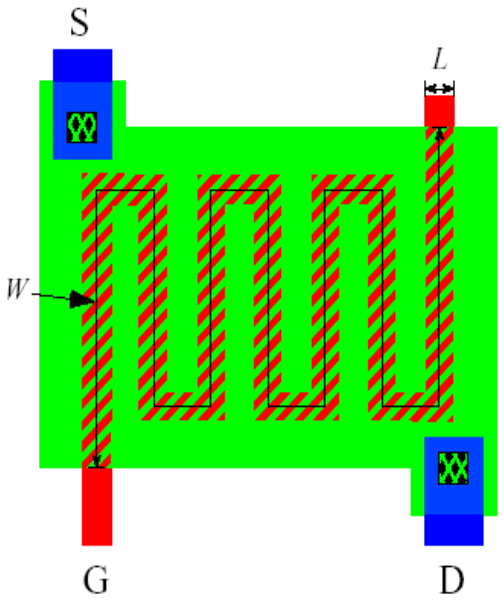
Transistoren in Reihe





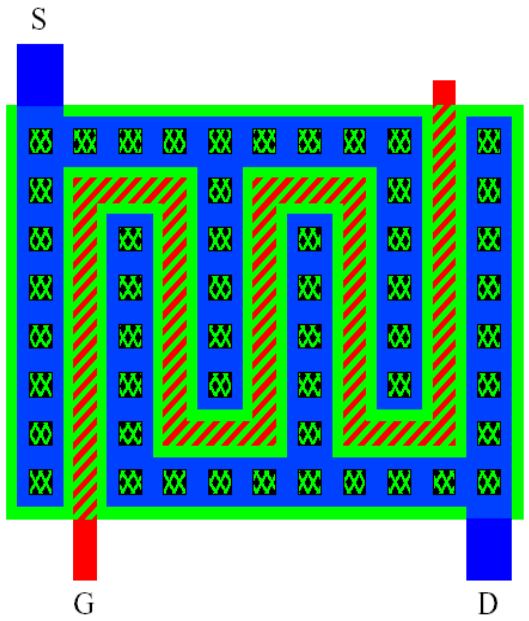
Out = A and B and C

Transistoren für höhere Drainströme (Gate ist serpentinenartig bzw. mäanderförmig ausgelegt)

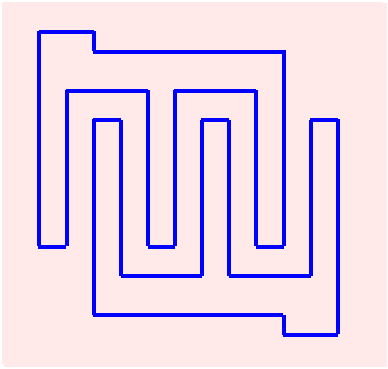


$W >> L$

Source and drain are interdigitated



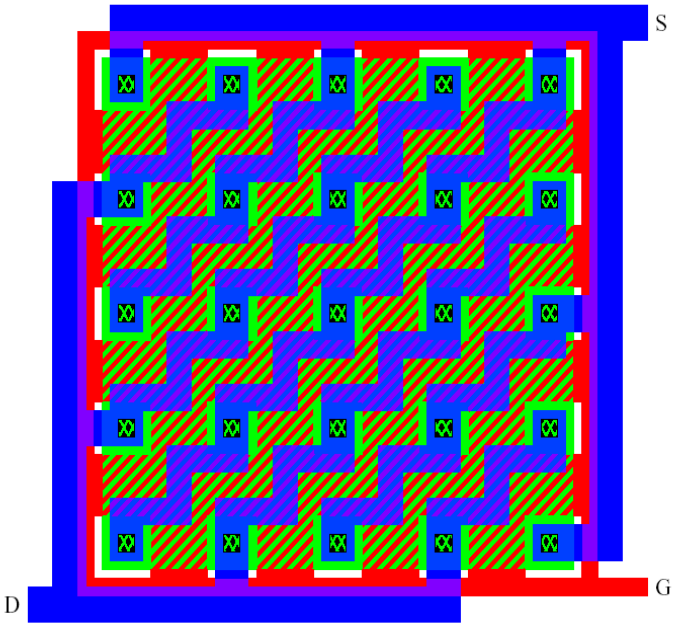
Interdigitalstruktur:



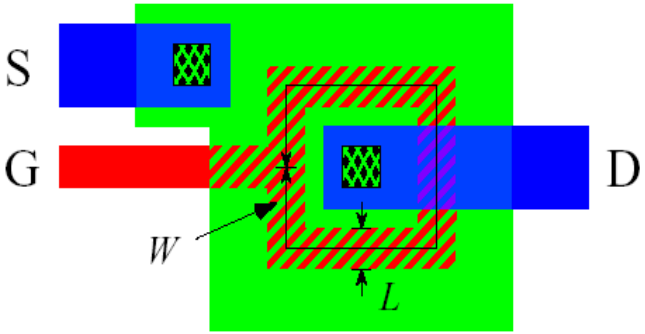
Minimize source and drain series resistance by using many contacts

Bauteile - FET

Waffle Transistors:
Ähnlich Stacked Transistors
- großes W/L Verhältnis bei vorgegebener Fläche
- kleine parasitäre S- und D-Kapazitäten
- geringe S-, D- und G- Widerstände
- besser: diagonale Linen, wenn erlaubt

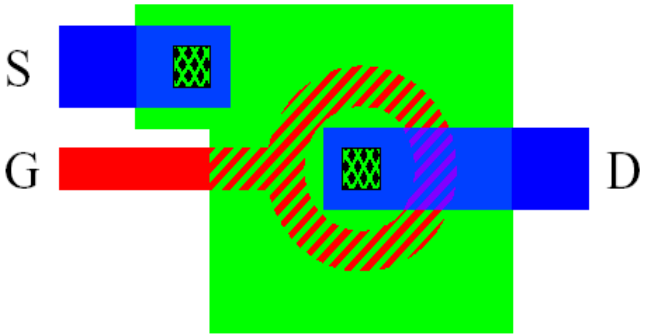


Andere Möglichkeit für großes W/L-Verhältnis: Ringtransistoren



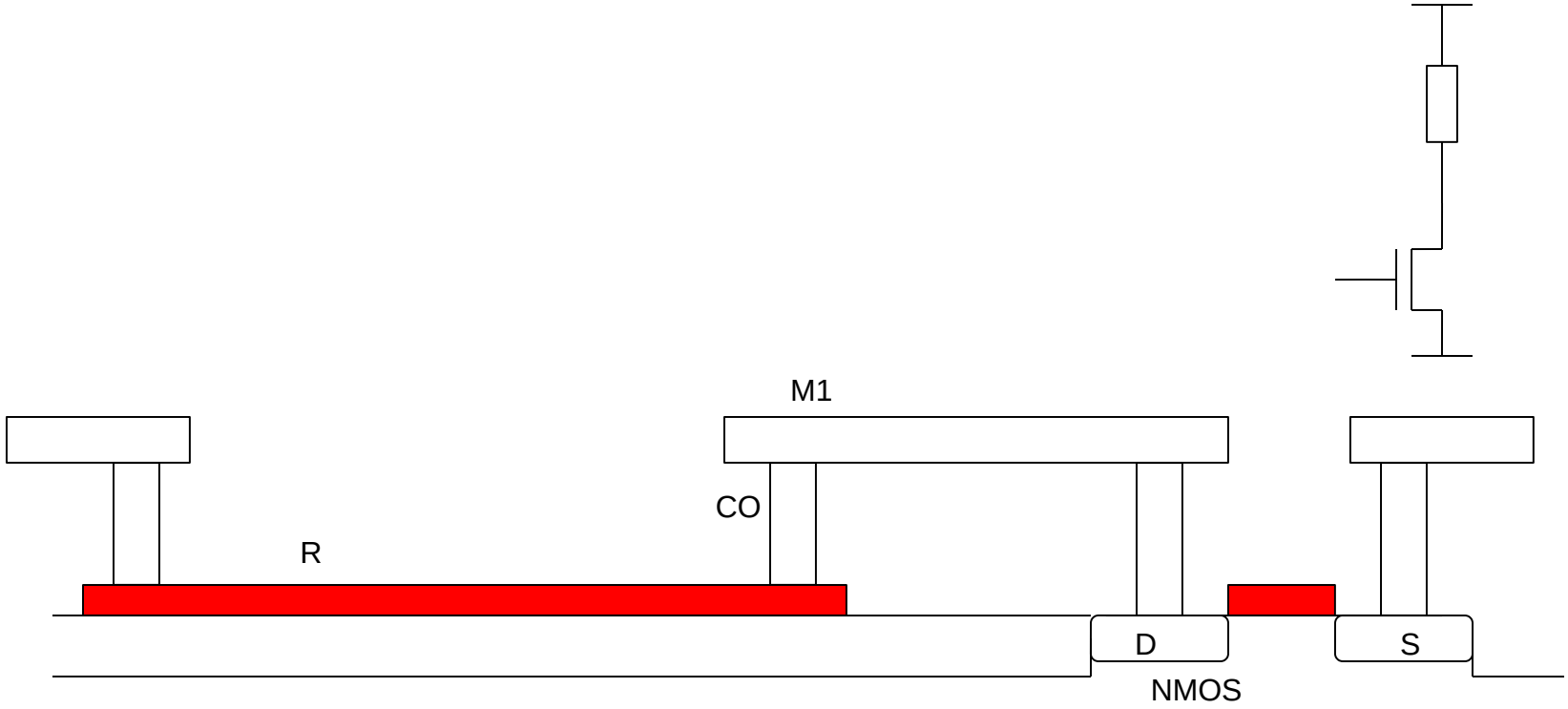
Vorteile: maximale W/L-Verhältnis für eine vorgegebene Maximale Drainkapazität

Kanal besitzt keine "Enden", dadurch treten diese Randeffekte nicht auf

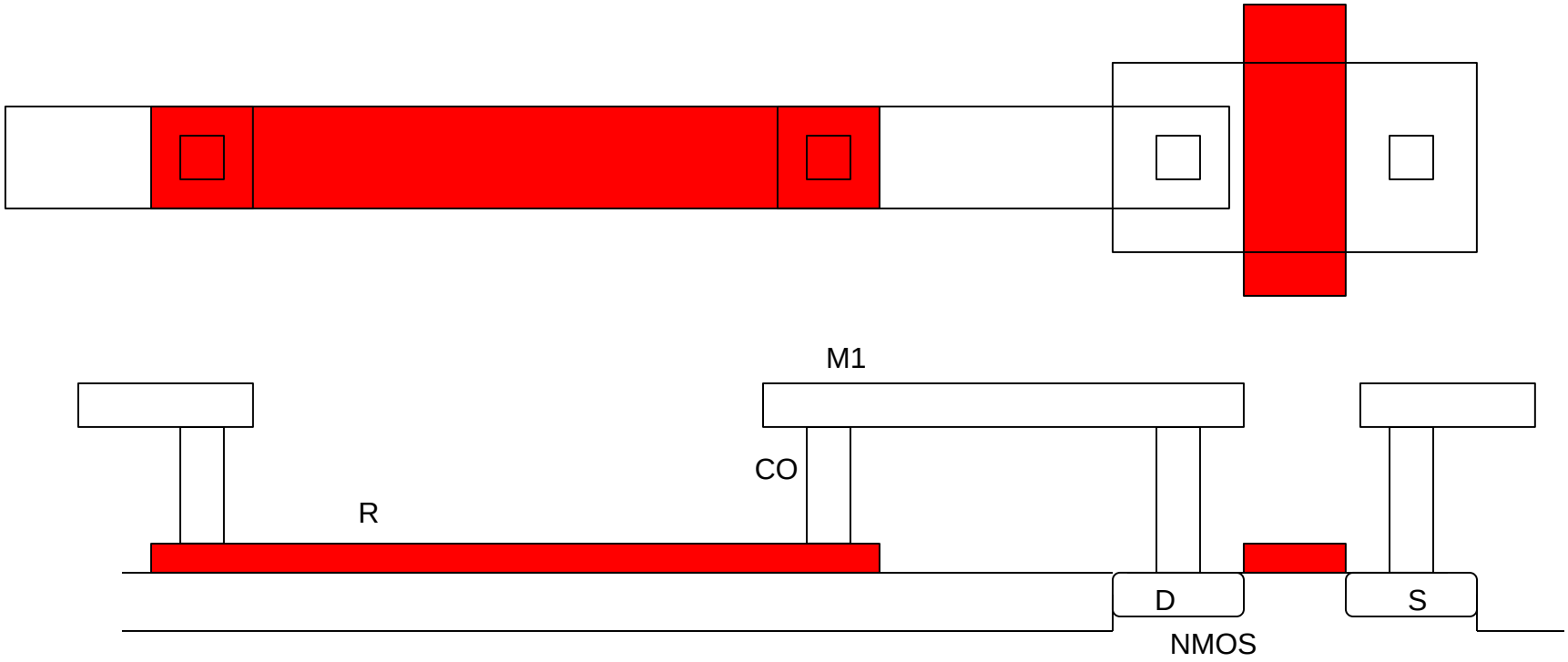


Beste Lösung: kreisförmiger Kanal, da hier ein gleichmäßiger Abstand zwischen Source und Drain und damit eine konstante Kanallänge garantiert ist. (Allerdings nicht bei allen Entwürfen erlaubt)

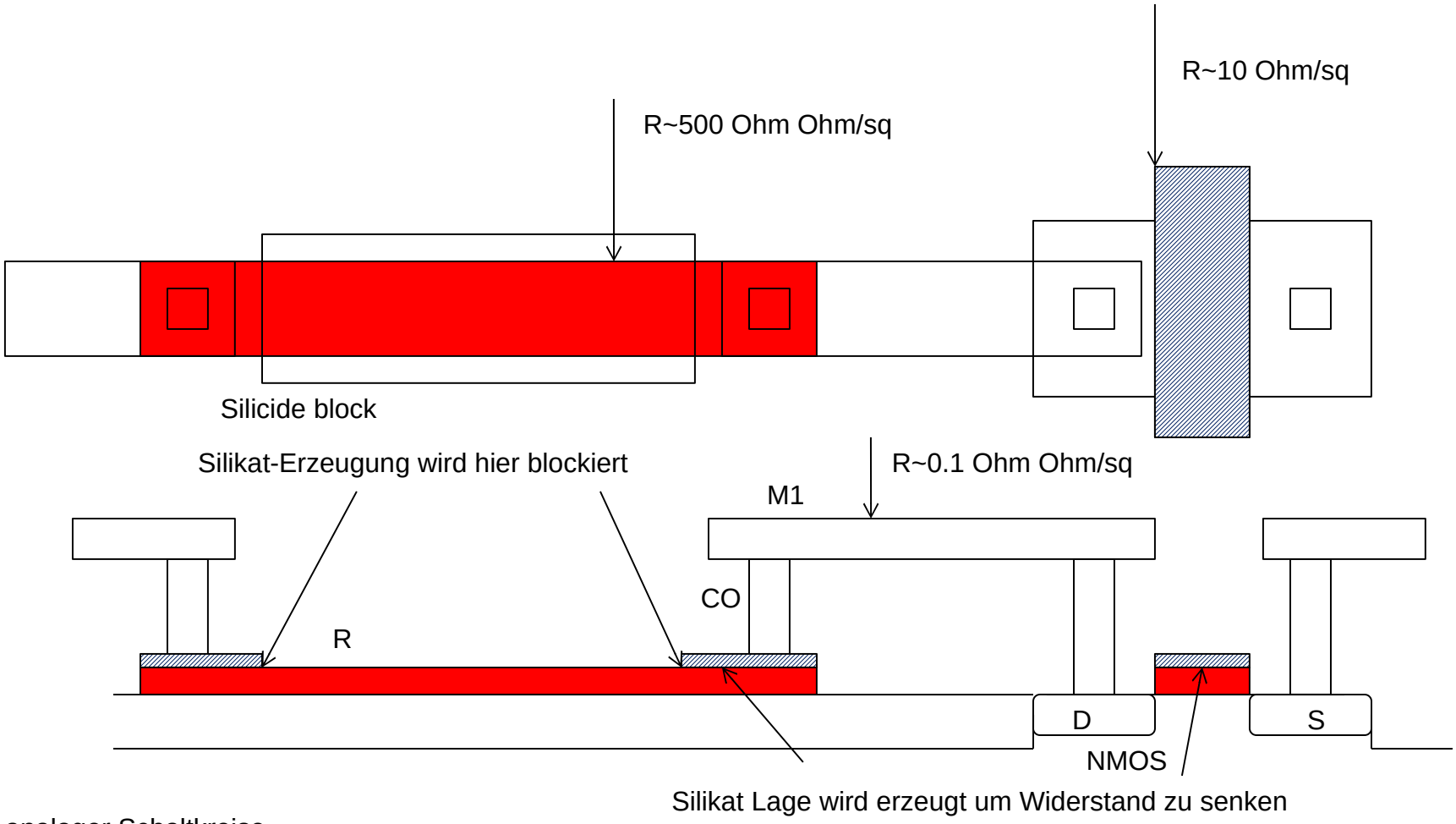
Bauteile – Poly-Widerstand



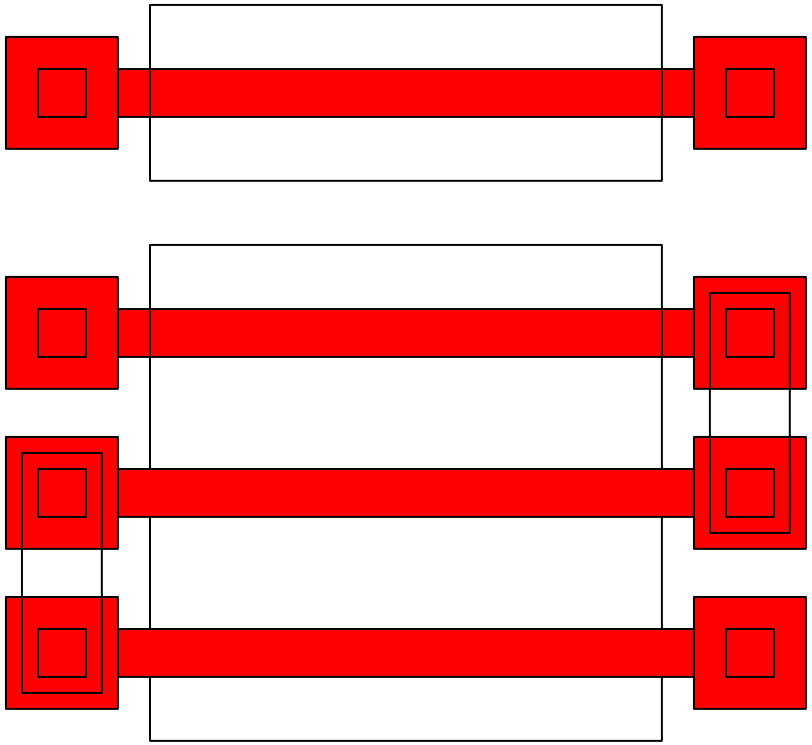
Bauteile – Poly-Widerstand



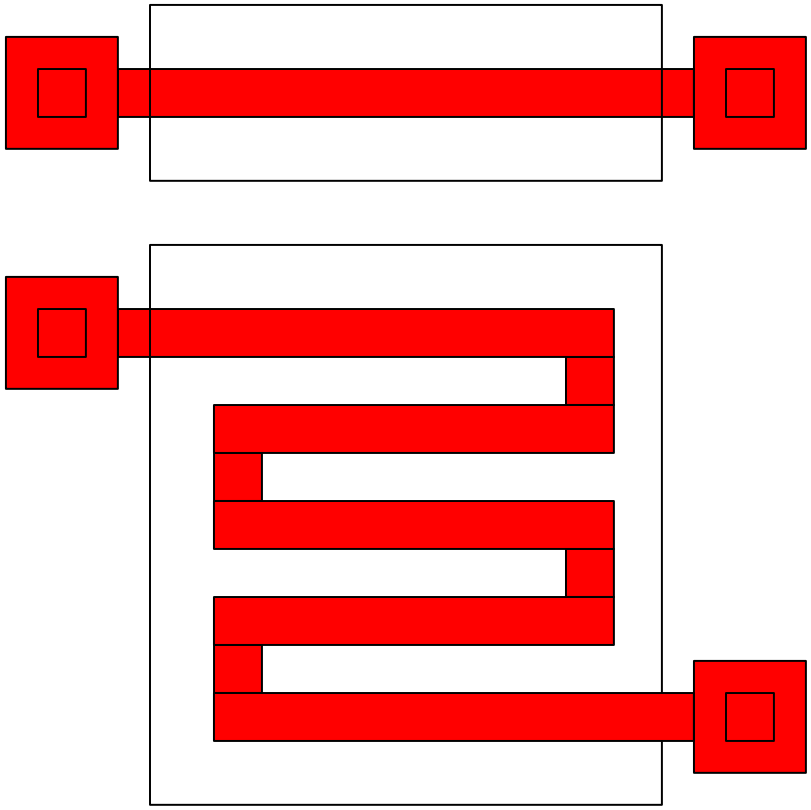
Bauteile – Poly-Widerstand



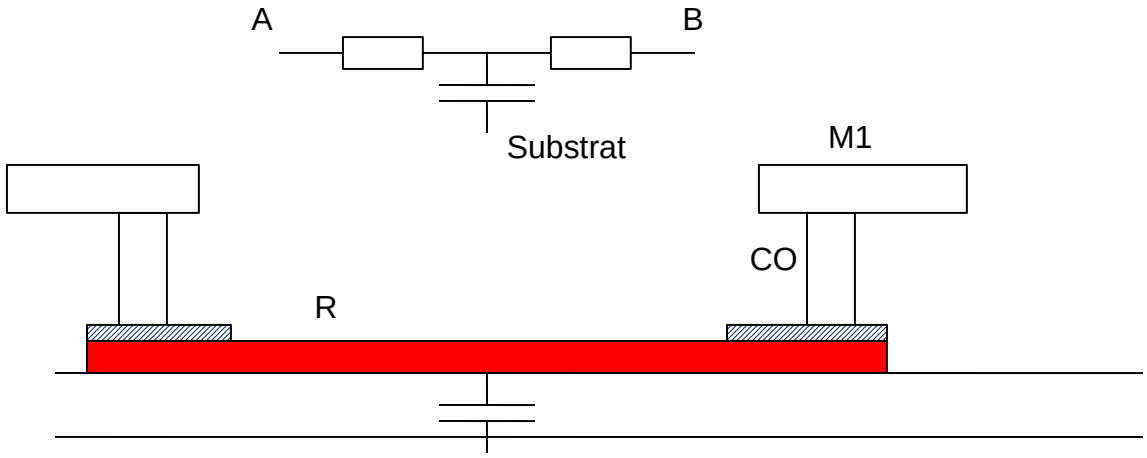
Bauteile – Poly-Widerstand



Bauteile – Poly-Widerstand

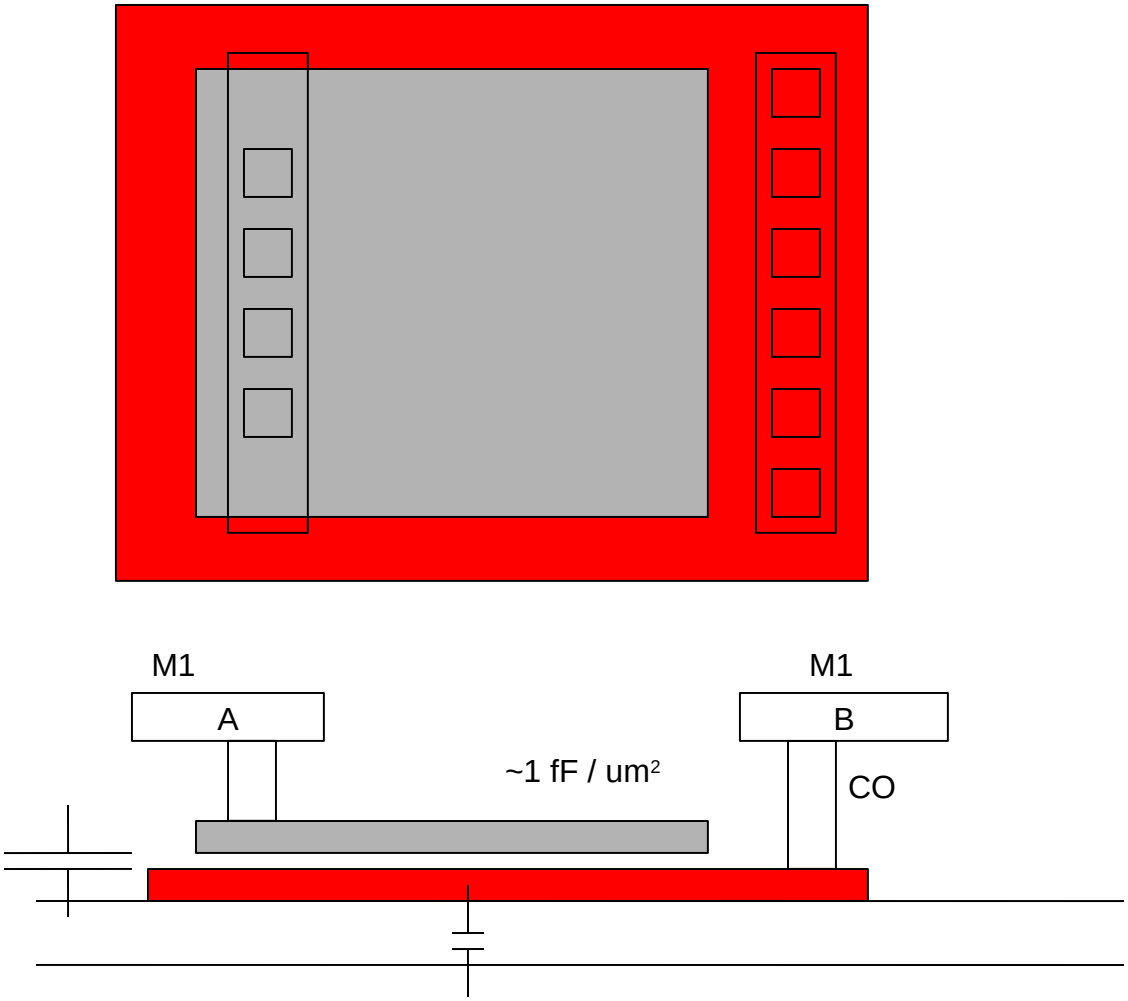


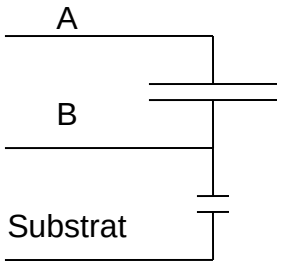
Bauteile – Poly-Widerstand



Bauteile – Kondensator

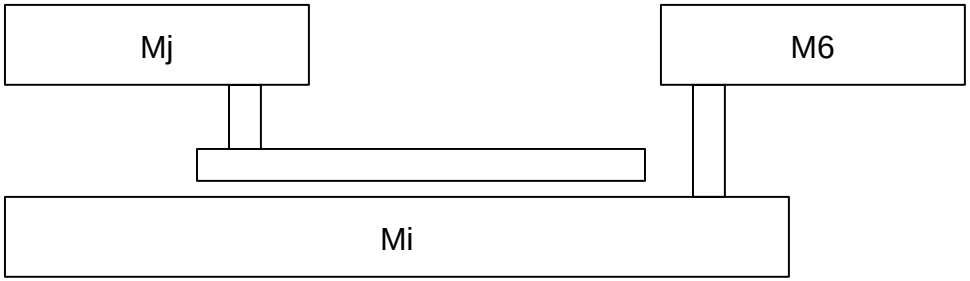
- Poly-Poly Kondensator

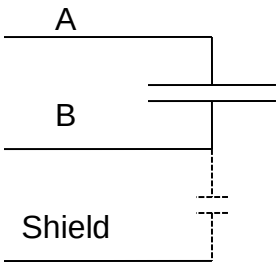


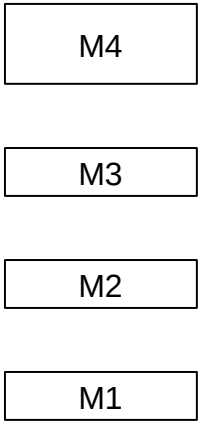


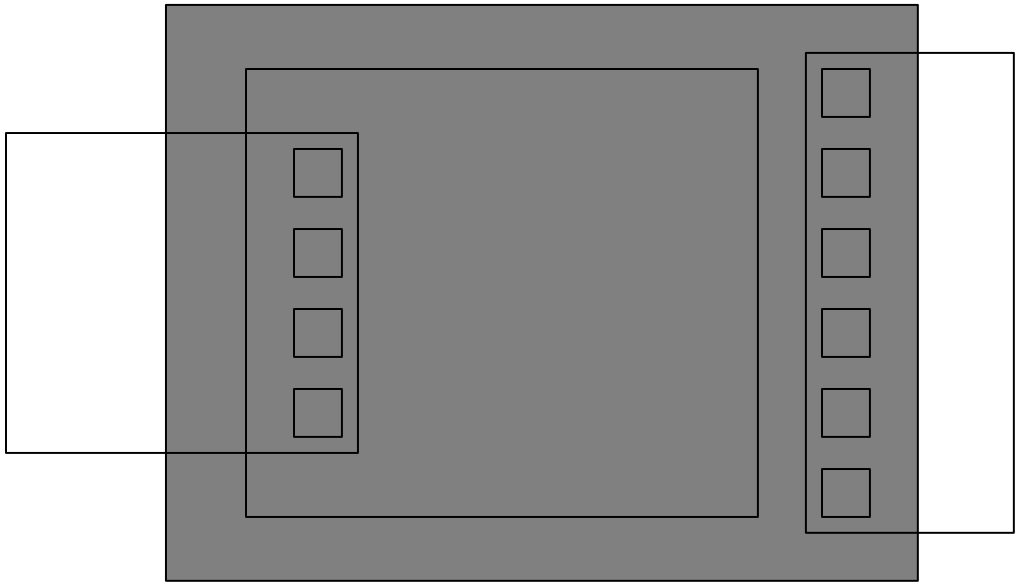
Bauteile – Kondensator

- Metal-Metal Kondensator



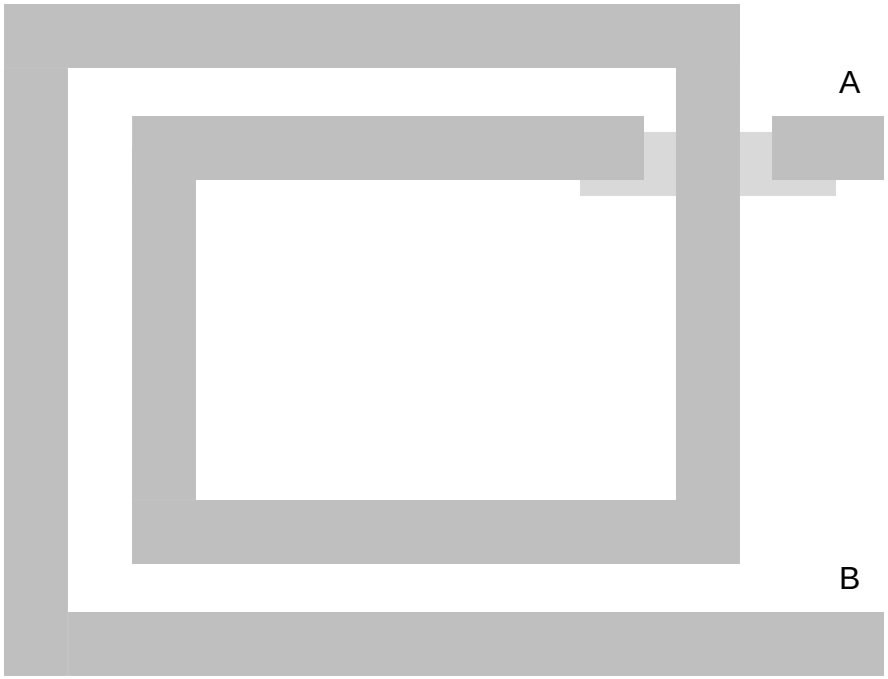




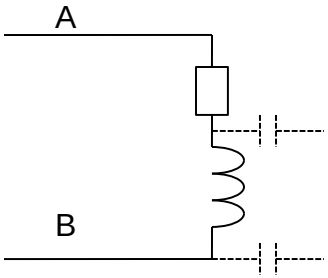


Bauteile – Induktor

- Induktor



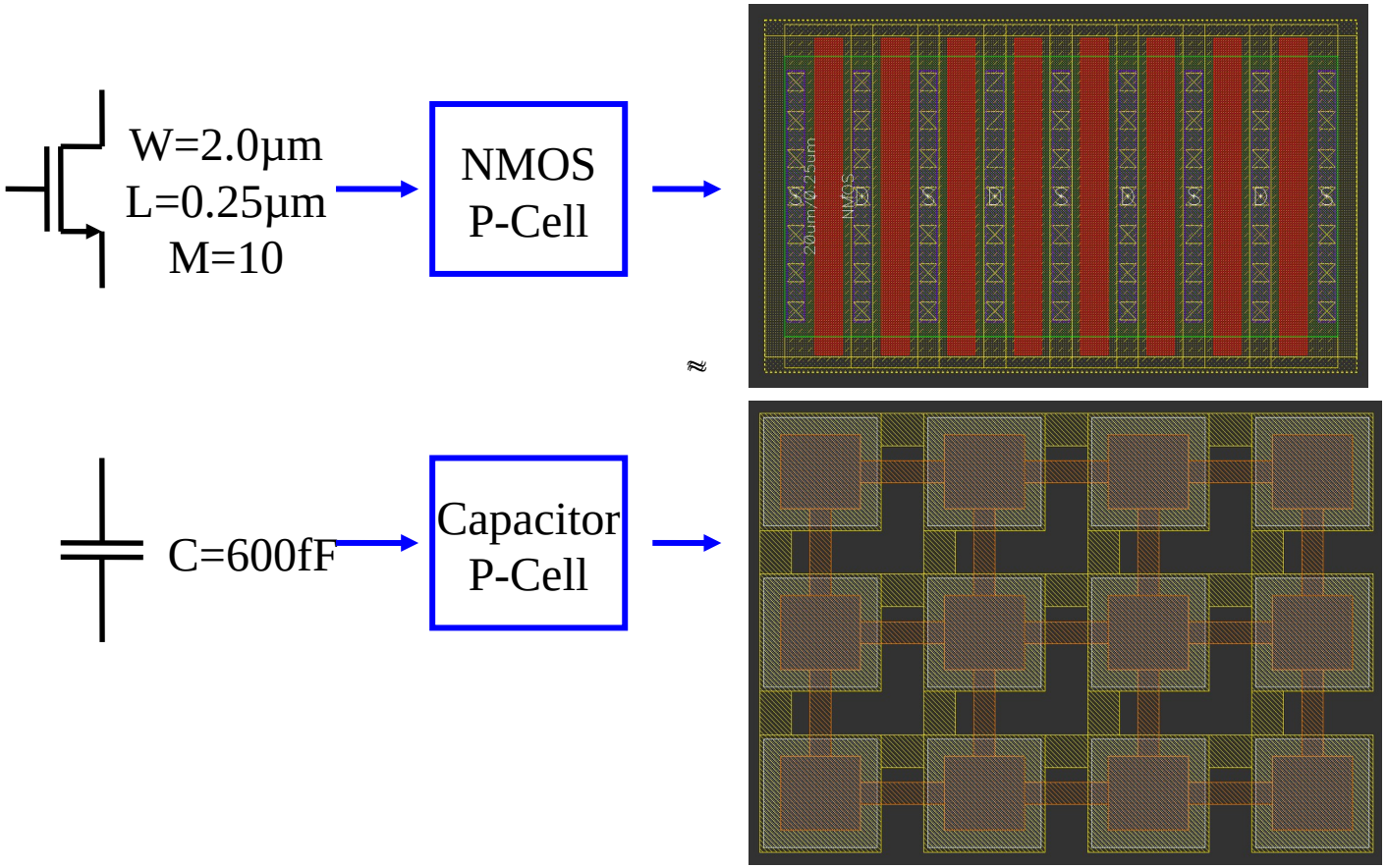
Letzte Metalllage – niedrigster Widerstand



Designablauf

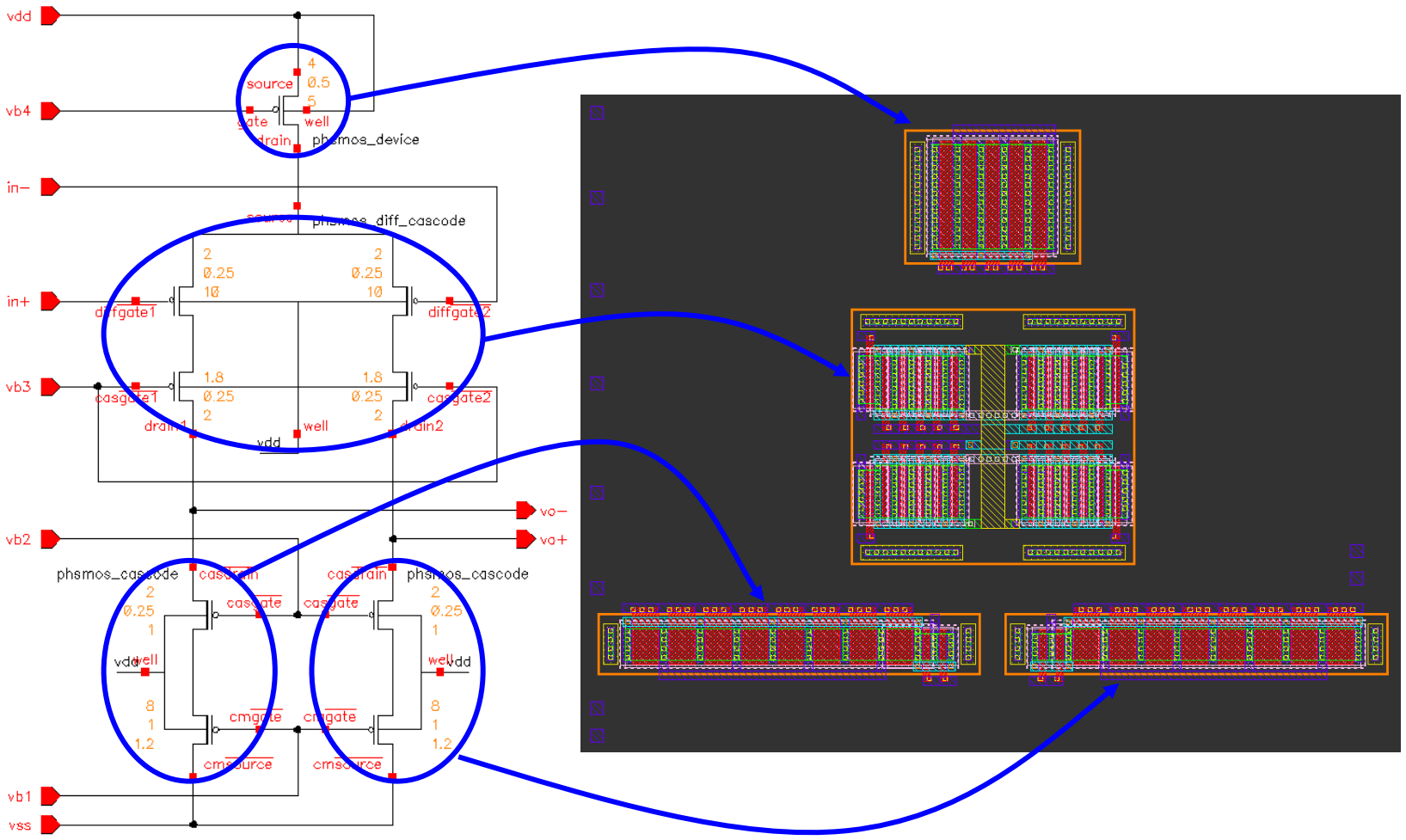
Layout-Designablauf

Parametrisierte Zellen
Durch Zuweisung von Werten können die Layouts angepasst werden

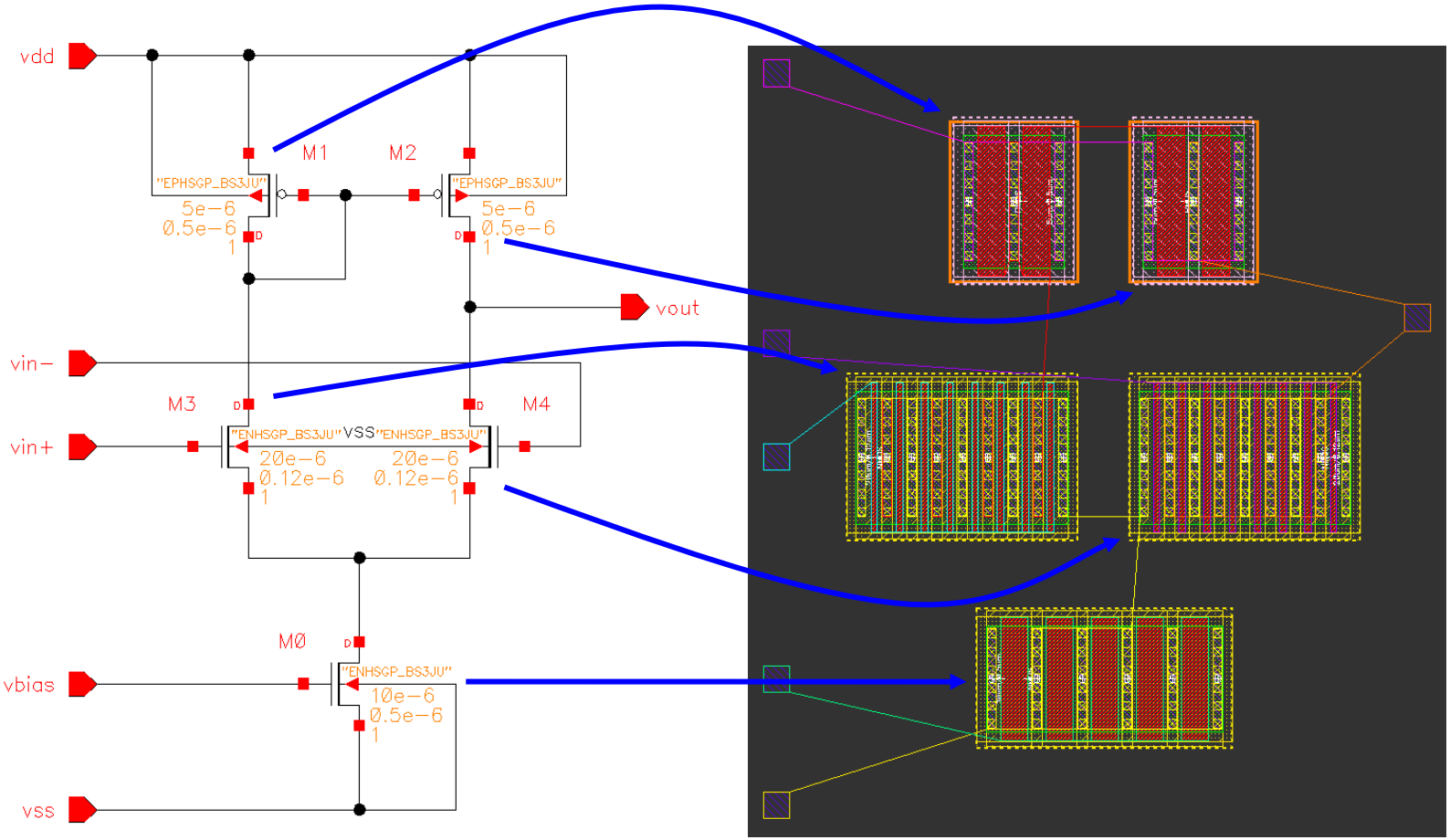


Layout-Designablauf

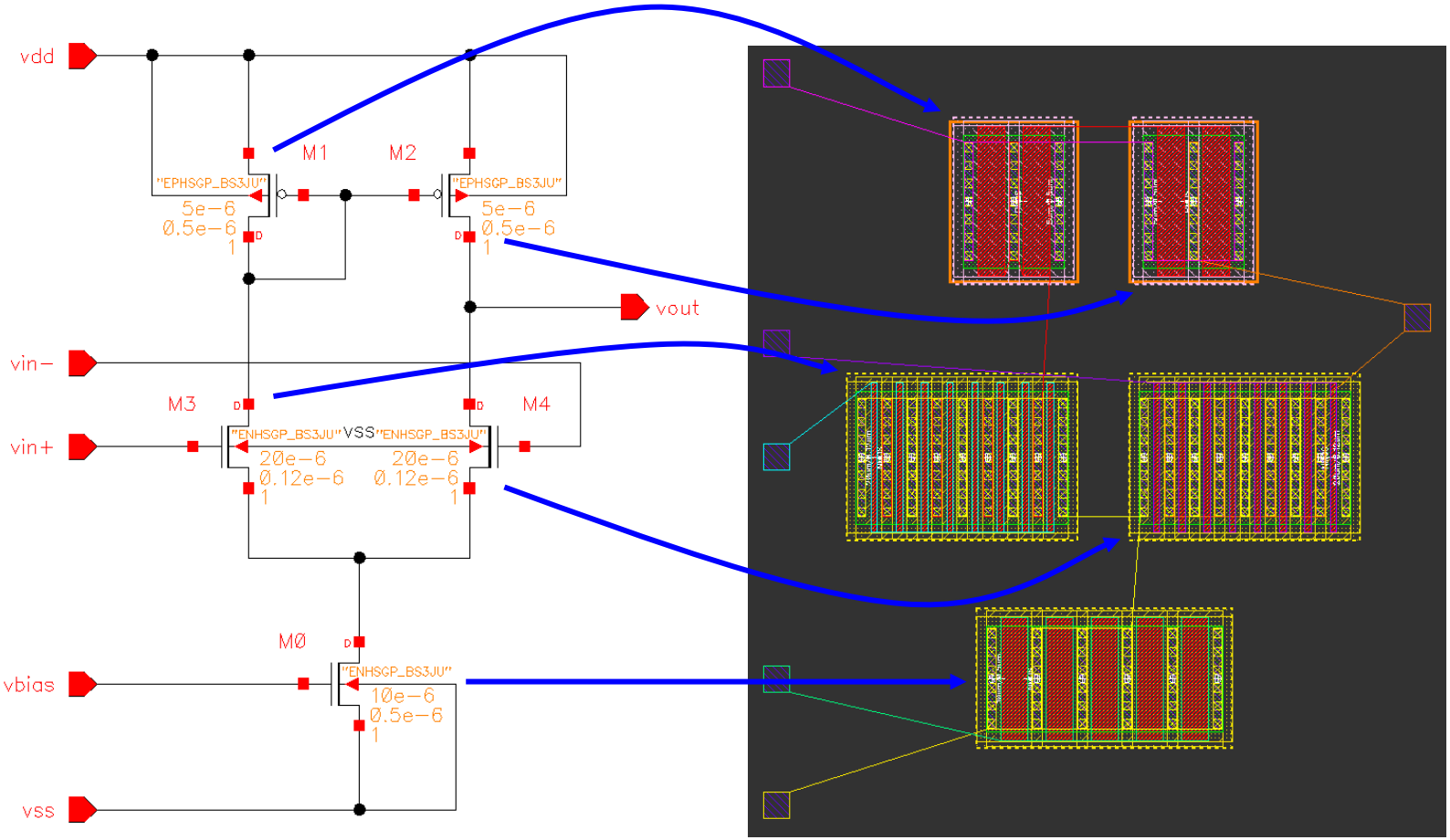
Bauelemente als P-Zellen werden platziert (automatisch oder per Hand)



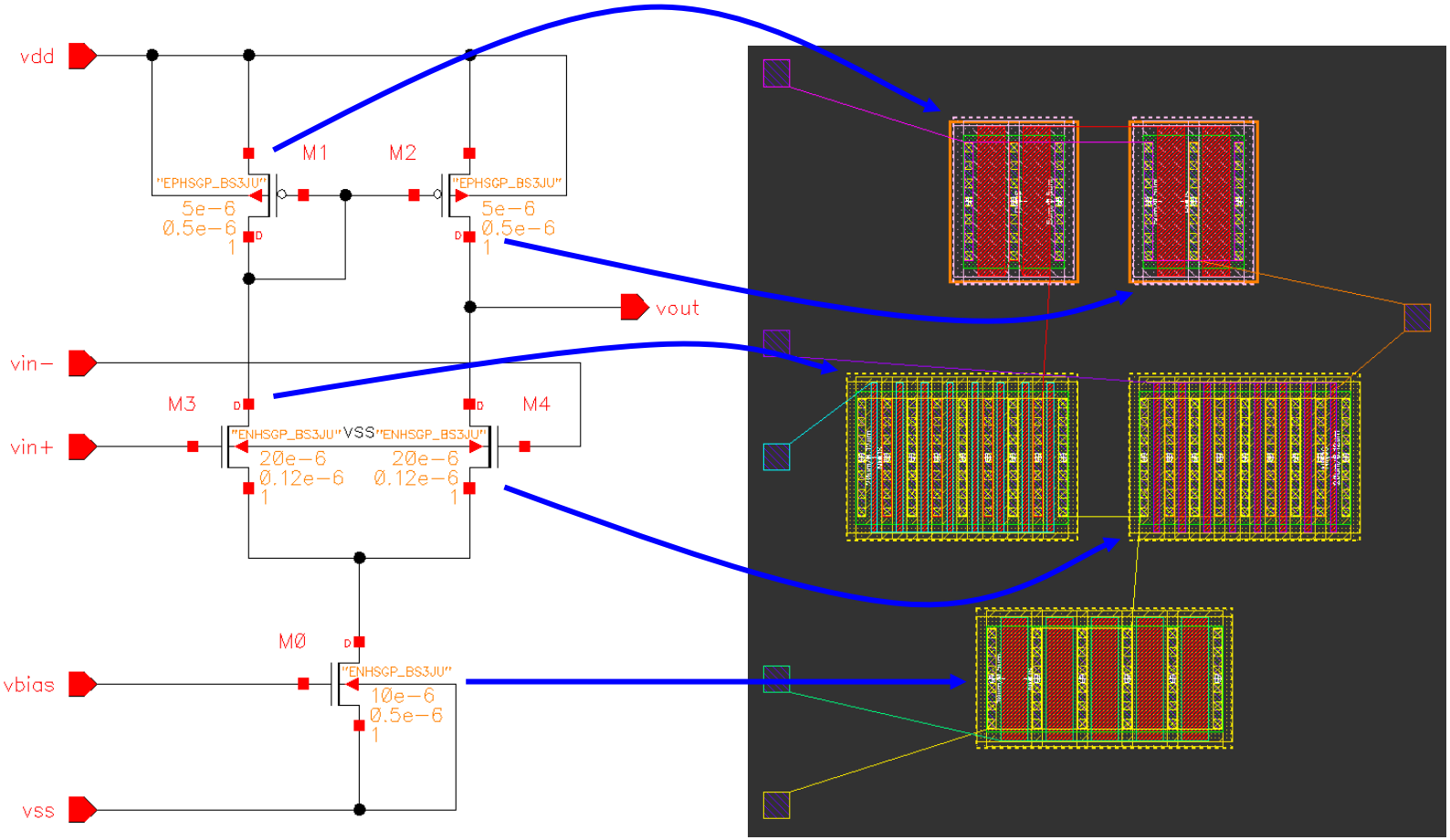
Cadence Design Systems: Virtuoso XL
Bauelemente und Pins werden wie im Schaltplan angegeben platziert



Bauelemente werden mit Metalllagen verbunden



Design Rule Check (DRC) - Tool



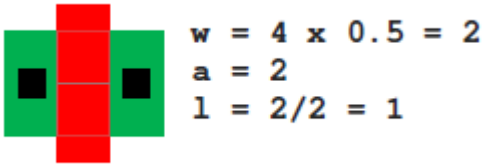
Layout-Designablauf

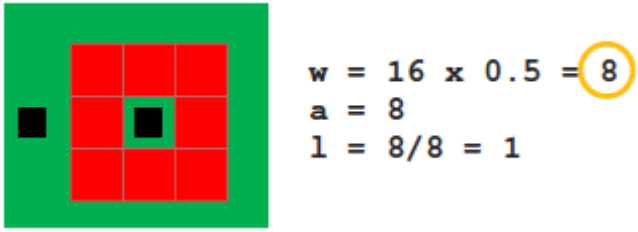
- Layout versus Shematic Tool (LVS)
- 3 Schritte
- 1. Netzliste wird aus dem Schaltplan extrahiert
- 2. Netzliste wird aus dem Layout extrahiert
- Vergleich von Netzlisten
- Bauelemente und Netze dürfen verschiedene Namen haben
- Algorithmen sind kompliziert
- 1:1 Übereinstimmung ist nicht notwendig
- Z.B. Reihenfolge bei Serienschaltungen unwichtig, Source und Drain vertauschbar, Reihen- und Parallelschaltungen zusammengeführt

Layout-Designablauf

- Extraction Tool
- 1. Erkennt Transistoren und Bauelemente

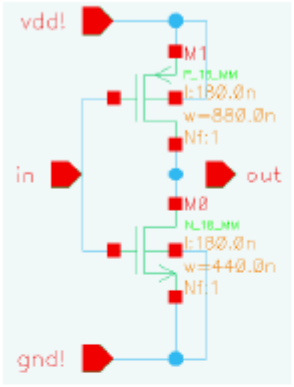
- 2. Bestimmt die geometrische Parameter: W, L, Source/Drain Flächen
- Beispiel: Programmiersprache „Skill“
- W = measureParameter (length (gate coincident poly) 0.5e-6)
- A = measureParameter (area (gate) 1.0e-12)
- L = calculateParameter (a / L)





- LVS

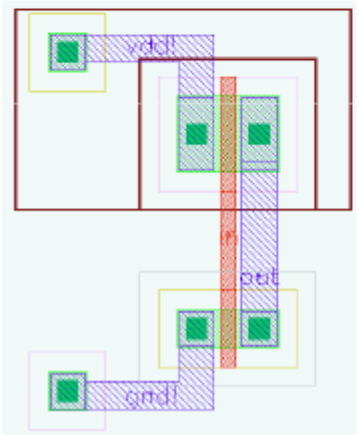
Schematic



Extracted schematic netlist:

```
* 2 instances
i M1 P_18_MM out  in vdd! vdd!
  L 1.8e-07  M 1 W 8.8e-07
i M0 N_18_MM out  in gnd! gnd!
  L 1.8e-07  M 1 W 4.4e-07
```

Layout

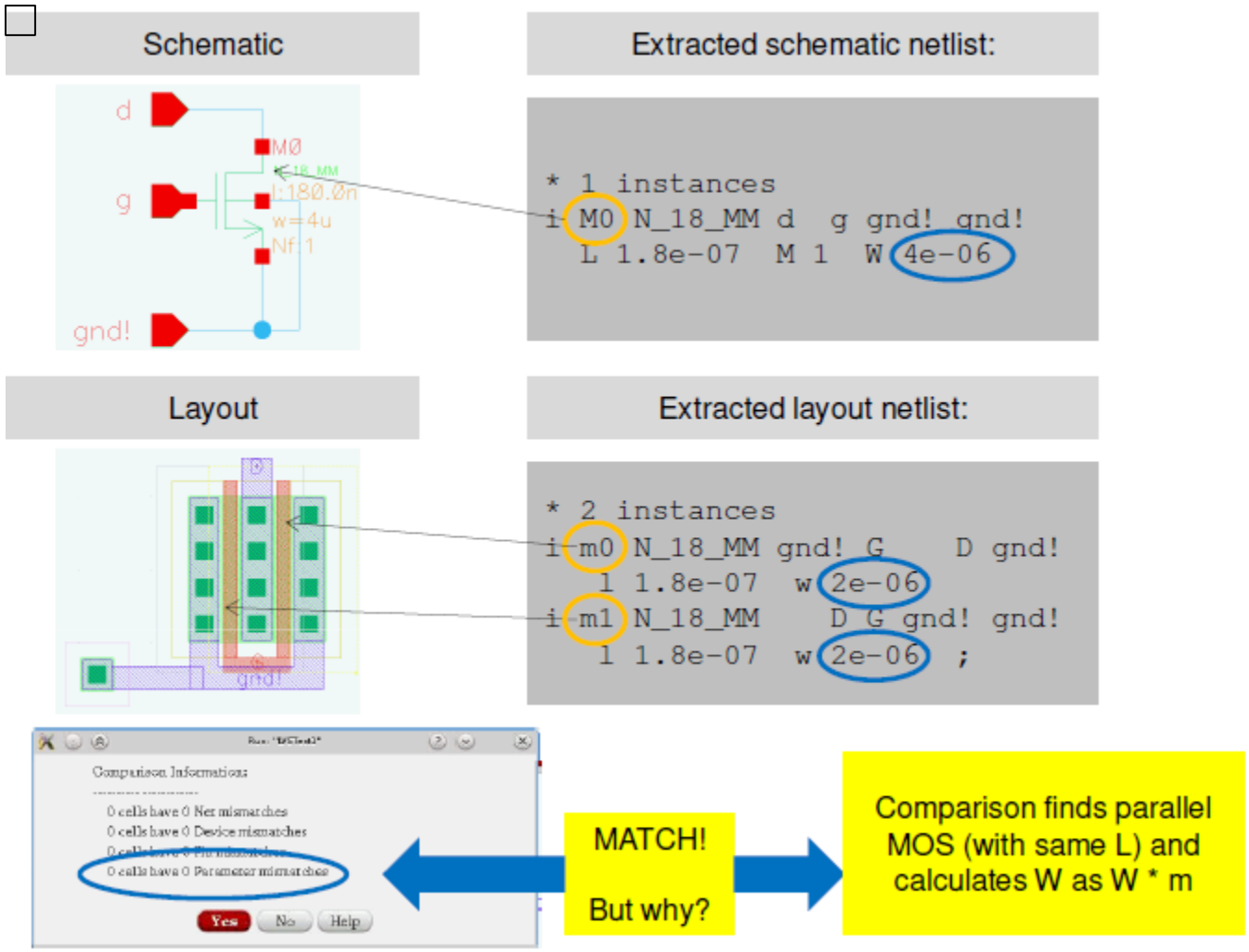


Extracted layout netlist:

```
* 2 instances
i av1 N_18_MM out in gnd! gnd!
  l 1.8e-07  w 4.4e-07;
i av2 P_18_MM out in vdd! vdd!
  l 1.8e-07  w 8.8e-07;
```

Layout-Designablauf

- LVS



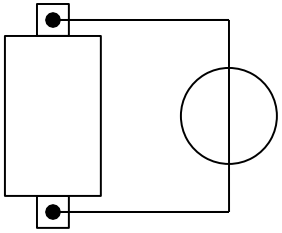
Matching

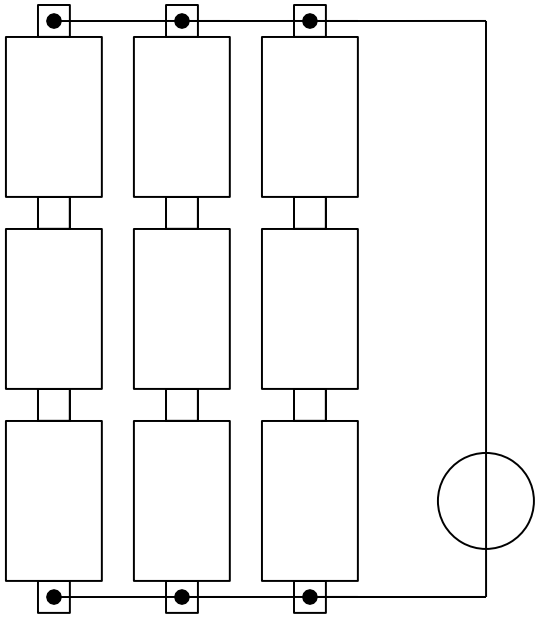
$$I = U / R$$

Minus Vorzeichen werden wir vernachlässigen

$$dI = \frac{U}{R^2} dR = I \frac{dR}{R}$$

$$\sigma(I) = I \frac{\sigma(R)}{R}$$





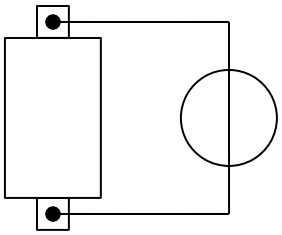
Matching

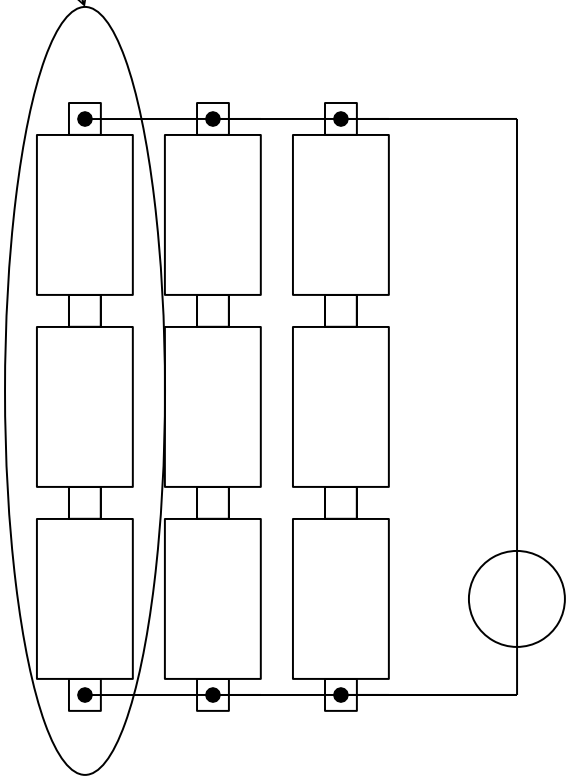
$$I = U / R$$

$$dI = \frac{U}{R^2} dR = I \frac{dR}{R}$$

$$\sigma(I) = I \frac{\sigma(R)}{R}$$

$$I = U \sum_{i=1}^{N} \frac{1}{\sum_{j=1}^{N} R_{ji}} = U \frac{N}{N} \frac{1}{R_{ij}} = \frac{U}{R}$$





Matching

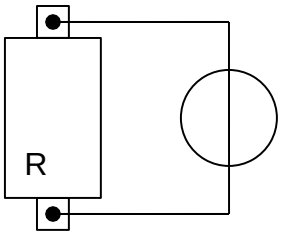
$$I = U / R$$

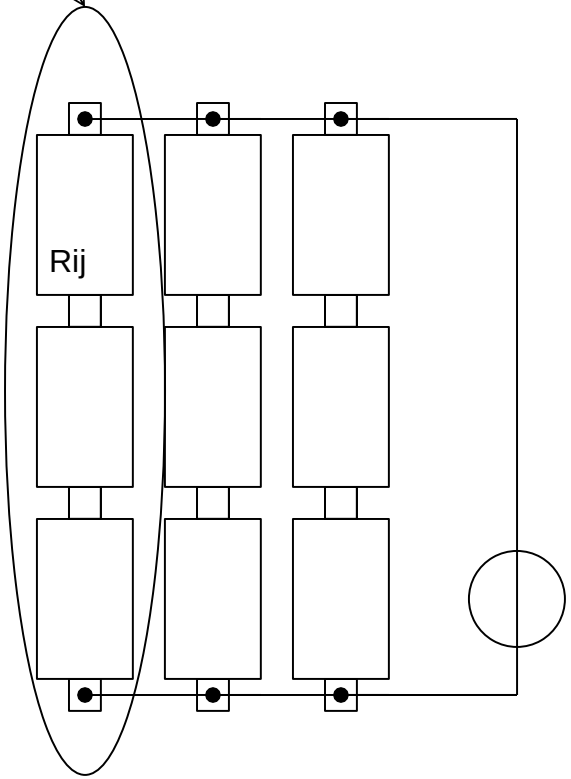
$$dI = \frac{U}{R^2} dR = I \frac{dR}{R}$$

$$\sigma(I) = I \frac{\sigma(R)}{R}$$

$$I = U \sum_{i=1}^{N} \frac{1}{\sum_{j=1}^{N} R_{ji}} = U \frac{N}{N} \frac{1}{R_{ij}} = \frac{U}{R}$$

$$dI = U \sum_{i=1}^{N} \frac{\sum_{j=1}^{N} dR_{ji}}{\left(\sum_{j=1}^{N} R_{ji} \right)^2} = U \frac{\sum_{i=1}^{N} \sum_{j=1}^{N} dR_{ji}}{N^2 R^2}$$





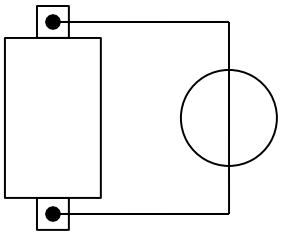
$$I = U / R$$

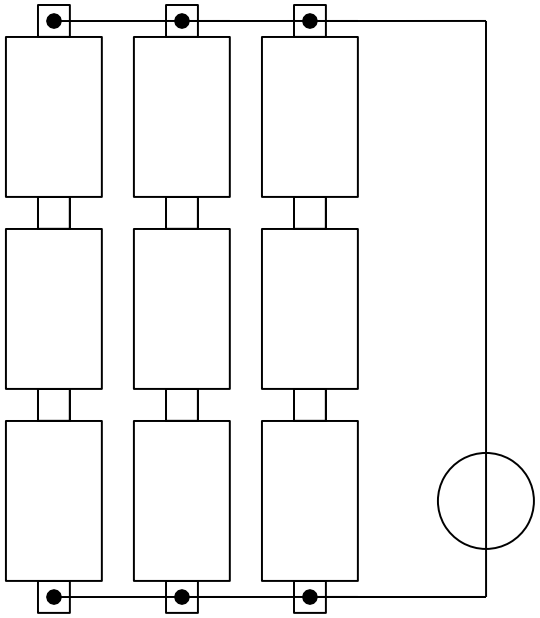
$$dI = \frac{U}{R^2} dR = I \frac{dR}{R}$$

$$\sigma(I) = I \frac{\sigma(R)}{R}$$

$$dI = U \sum_{i=1}^{N} \frac{\sum_{j=1}^{N} dR_{ji}}{\left(\sum_{j=1}^{N} R_{ji} \right)^2} = U \frac{\sum_{i=1}^{N} \sum_{j=1}^{N} dR_{ji}}{N^2 R^2}$$

$$\sigma^2(I) = \left(\frac{U}{N^2 R^2} \right)^2 \sum_{i=1}^{N} \sum_{j=1}^{N} \sigma^2(R) = \frac{U^2}{R^2} \frac{N^2 \sigma^2(R)}{N^4}$$





$$I = U / R$$

$$dI = \frac{U}{R^2} dR = I \frac{dR}{R}$$

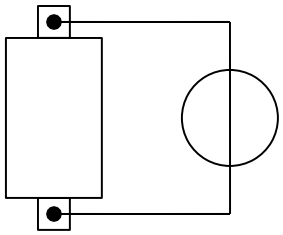
$$\sigma(I) = I \frac{\sigma(R)}{R}$$

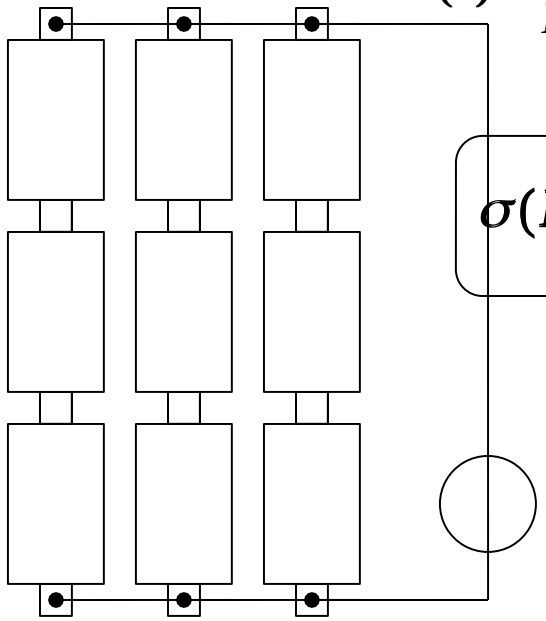
$$dI = U \sum_{i=1}^{N} \frac{\sum_{j=1}^{N} dR_{ji}}{\left(\sum_{j=1}^{N} R_{ji} \right)^2} = U \frac{\sum_{i=1}^{N} \sum_{j=1}^{N} dR_{ji}}{N^2 R^2}$$

$$\sigma^2(I) = \left(\frac{U}{N^2 R^2} \right)^2 \sum_{i=1}^{N} \sum_{j=1}^{N} \sigma^2(R) = \frac{U^2}{R^2} \frac{N^2 \sigma^2(R)}{N^4}$$

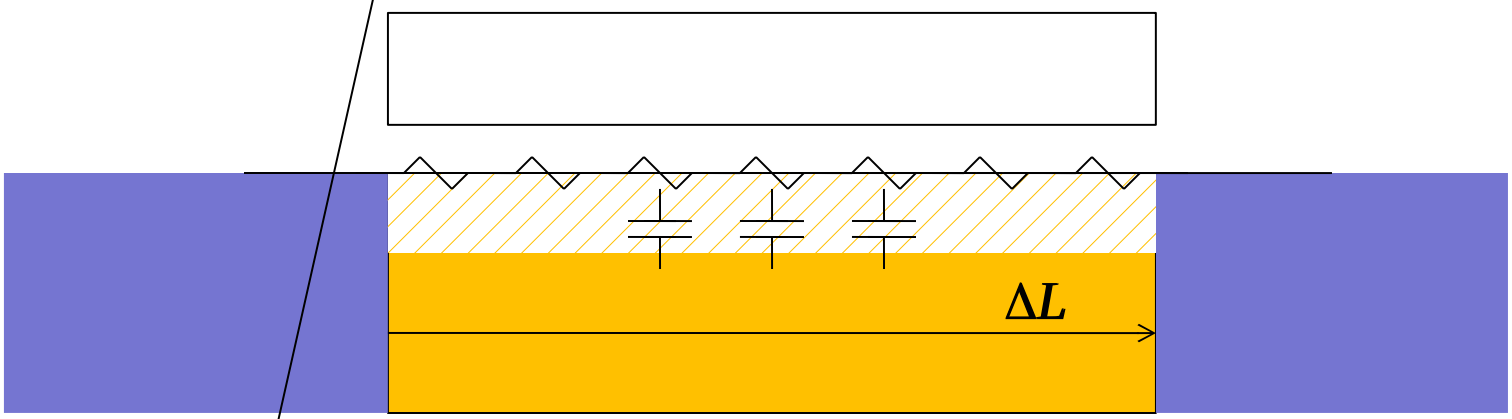
$$\sigma(I) = \frac{U}{R} \frac{\sigma(R)}{N} = I \frac{\sigma(R)}{RN}$$

$$\sigma(R_{ges}) = \frac{\sigma(R)}{N} \quad (1)$$





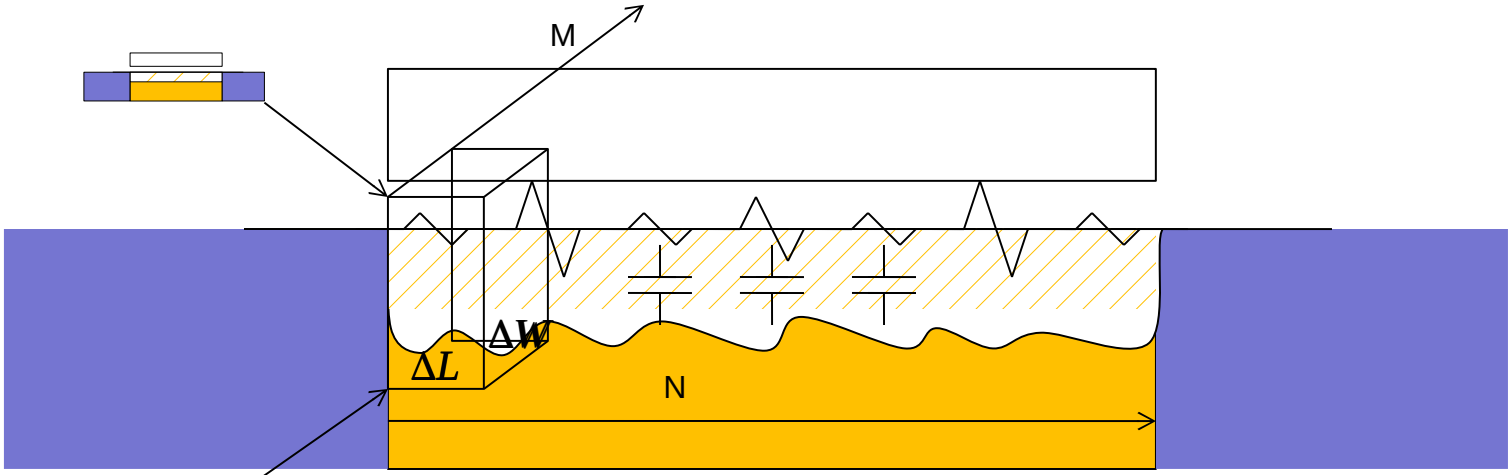
$$I_{ds} = \mu C'_{ox} \frac{\Delta W}{\Delta L}(V_{gs} - V_{th})V_{ds} \qquad V_{th} = \frac{C_{dep}}{C_{ox}}\psi$$



$$R = \frac{1}{\mu C'_{ox} \frac{\Delta W}{\Delta L}\frac{1}{2}(V_{gs} - V_{th})} \longrightarrow dR = R\frac{d\mu}{\mu} + R\frac{dV_{th}}{V_{gs} - V_{th}} \quad (2)$$

$$dI_{ds} = I_{ds}\frac{dR}{R} = I_{ds}\frac{d\mu}{\mu} + I_{ds}\frac{dV_{th}}{V_{gs} - V_{th}} \quad (3)$$

$$I_{ds} = \mu C'_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds} \qquad V_{th} = \frac{C_{dep}}{C_{ox}}\psi$$



$$R = \frac{1}{\mu C'_{ox} \frac{\Delta W}{\Delta L} \frac{1}{2}(V_{gs} - V_{th})}$$

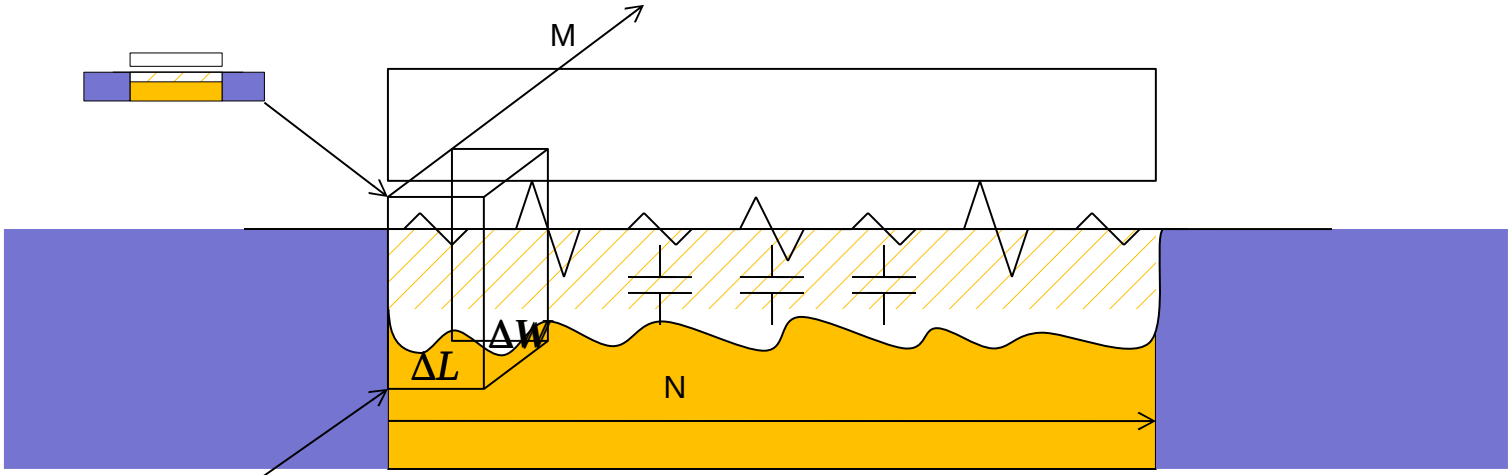
Aus Gl. (1) von Folie 65

$$\sigma(R_{ges}) = \frac{\sigma(R)}{\sqrt{NM}} \quad (4)$$

Aus Gl. (2) und (4)

$$\sigma(R_{ges}) = R\frac{\sigma(\mu)}{\sqrt{NM}\,\mu} + R\frac{\sigma(V_{th})}{\sqrt{NM}\,(V_{gs} - V_{th})} \quad (5)$$

$$I_{ds} = \mu C'_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds} \qquad V_{th} = \frac{C_{dep}}{C_{ox}}\psi$$

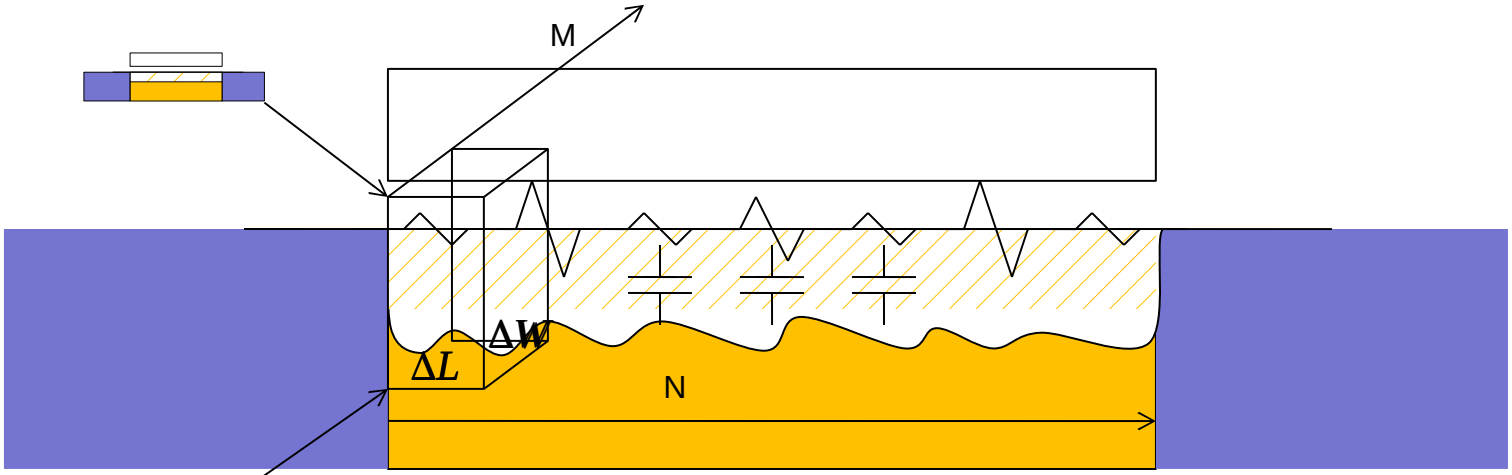


$$R = \frac{1}{\mu C'_{ox} \frac{\Delta W}{\Delta L} \frac{1}{2}(V_{gs} - V_{th})}$$

Aus Gl. (3) und (5)

$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{NM}} \frac{\sigma(\mu)}{\mu} + \frac{I_{ds}}{\sqrt{NM}} \frac{\sigma(V_{th})}{V_{gs} - V_{th}} \quad (6)$$

$$I_{ds} = \mu C'_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds} \qquad V_{th} = \frac{C_{dep}}{C_{ox}}\psi$$



$$R = \frac{1}{\mu C'_{ox} \frac{\Delta W}{\Delta L}\frac{1}{2}(V_{gs} - V_{th})}$$

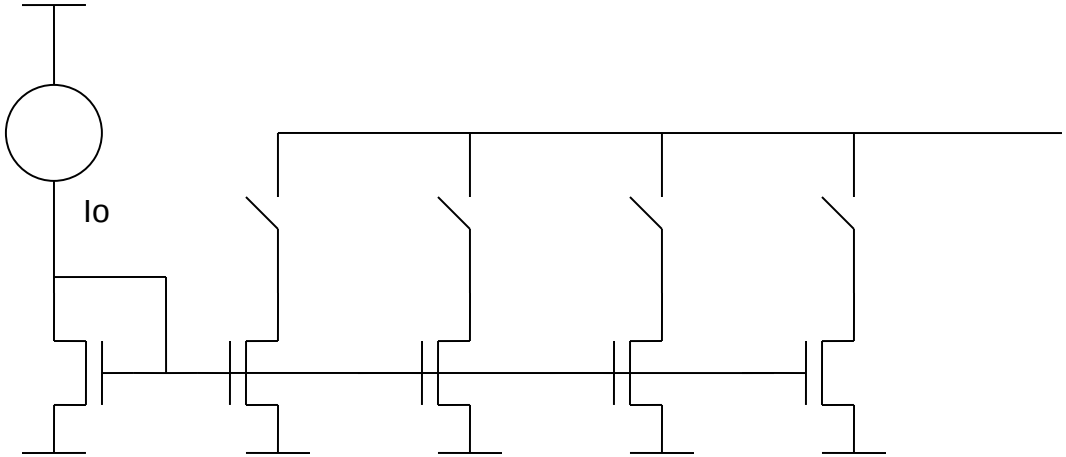
Aus Gl. (6)

$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(\mu)'}{\mu} + \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(V_{th})'}{V_{gs} - V_{th}}$$

$$\sigma(\mu)' = \sigma(\mu)\Delta L\Delta W, \quad \sigma(V_{th})' = \sigma(V_{th})\Delta L\Delta W$$

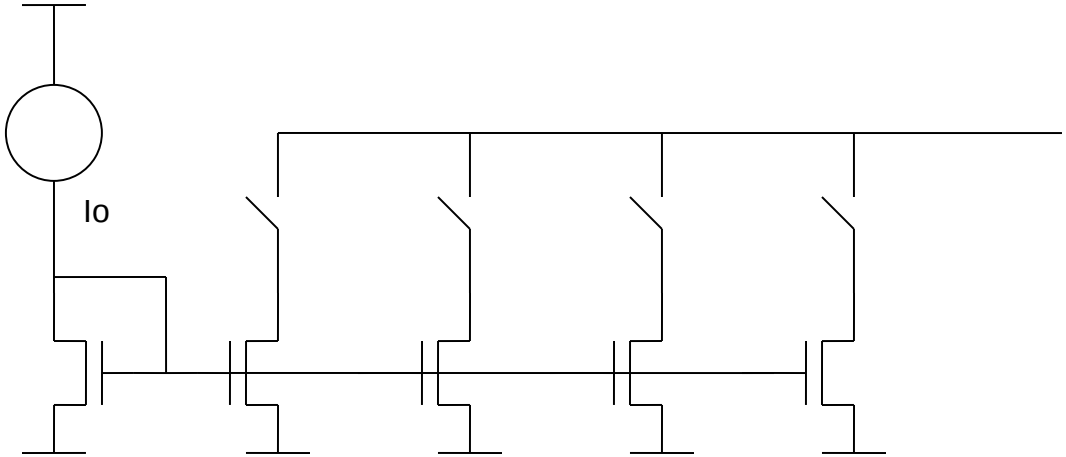
$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(\mu)'}{\mu} + \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(V_{th})'}{V_{gs} - V_{th}}$$

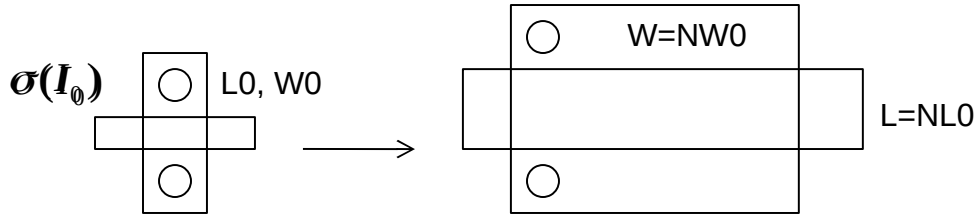
$$I_{ds} = \mu C'_{ox}\frac{W}{L}\frac{1}{2}(V_{gs} - V_{th})^2$$



$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(\mu)'}{\mu} + \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(V_{th})'}{V_{gs} - V_{th}}$$

$$I_{ds} = \mu C'_{ox}\frac{W}{L}\frac{1}{2}(V_{gs} - V_{th})^2$$

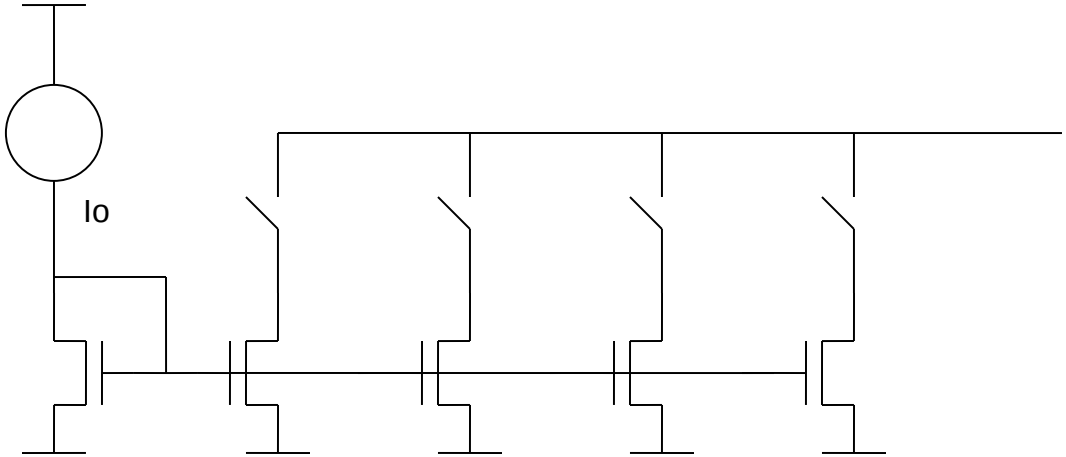




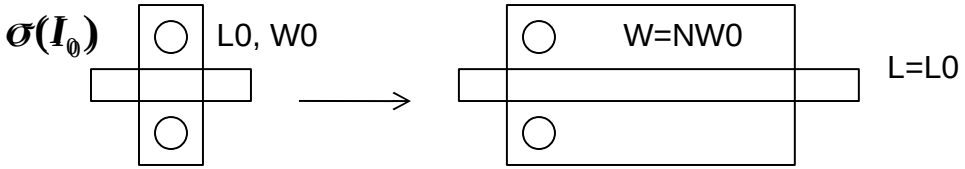
$$\sigma(I) = \frac{\sigma(I_0)}{N}$$

$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(\mu)'}{\mu} + \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(V_{th})'}{V_{gs} - V_{th}}$$

$$I_{ds} = \mu C'_{ox}\frac{W}{L}\frac{1}{2}(V_{gs} - V_{th})^2$$



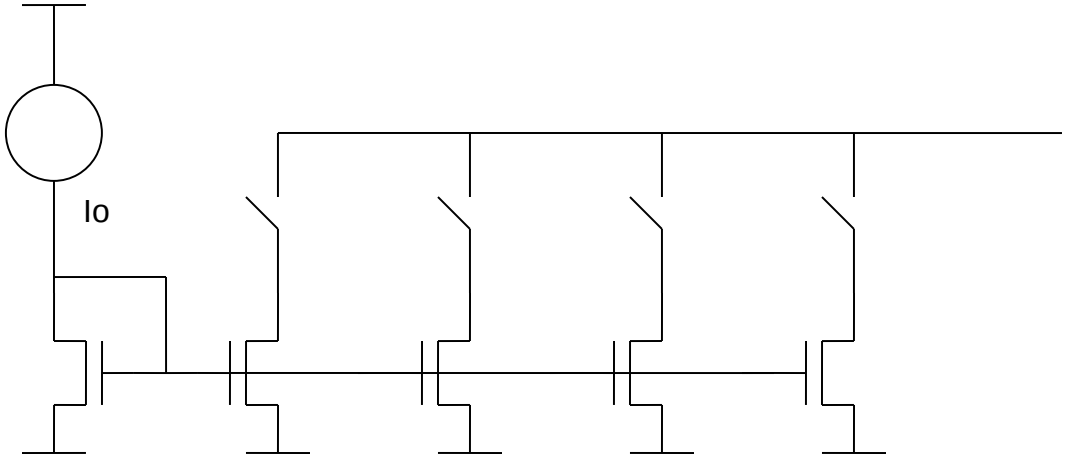
$$(V_{gs} - V_{th}) = (V_{gs} - V_{th})_0 / \sqrt{N}$$

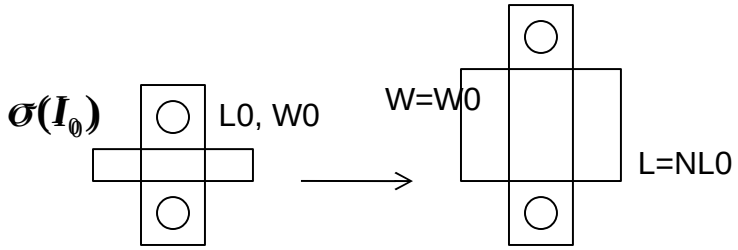


$$\sigma(I) \sim \sigma(I_0)$$

$$\sigma(I_{ds}) = \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(\mu)'}{\mu} + \frac{I_{ds}}{\sqrt{WL}}\frac{\sigma(V_{th})'}{V_{gs} - V_{th}}$$

$$I_{ds} = \mu C'_{ox}\frac{W}{L}\frac{1}{2}(V_{gs} - V_{th})^2$$

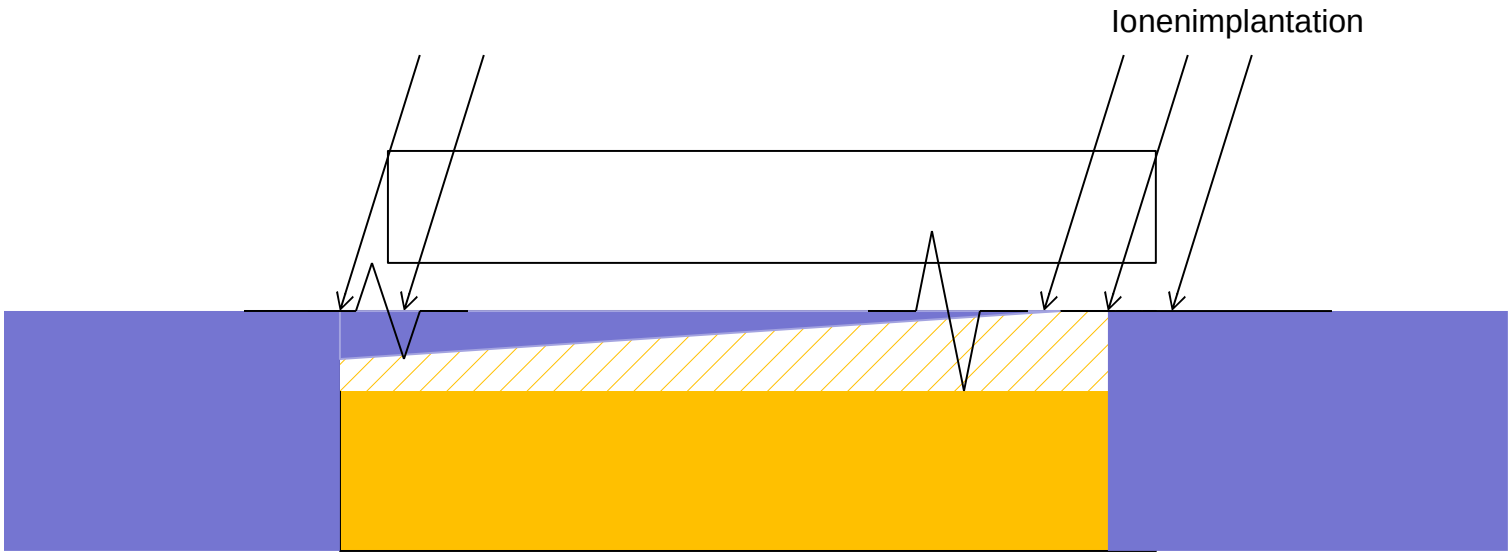


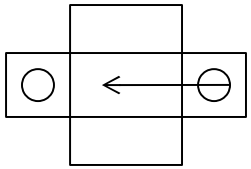


$$(V_{gs} - V_{th}) = \sqrt{N}(V_{gs} - V_{th})_0$$

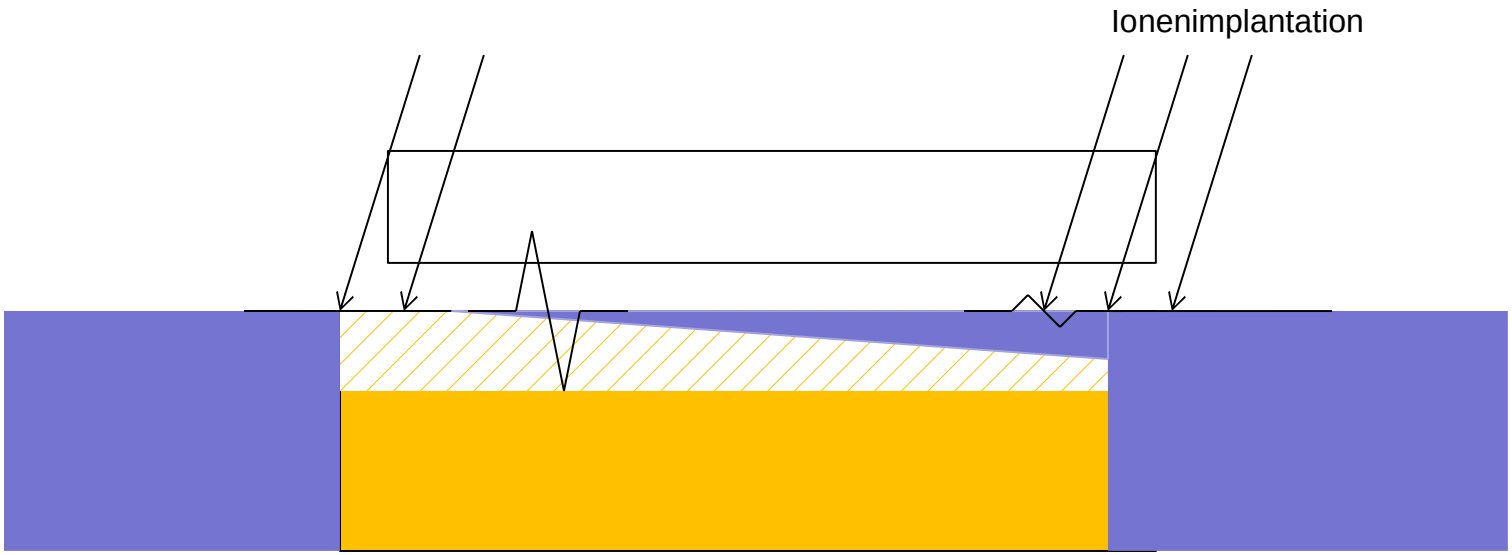
$$\sigma(I) = \sigma(I_0)/N$$

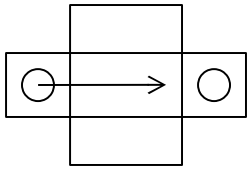
Matching





Matching

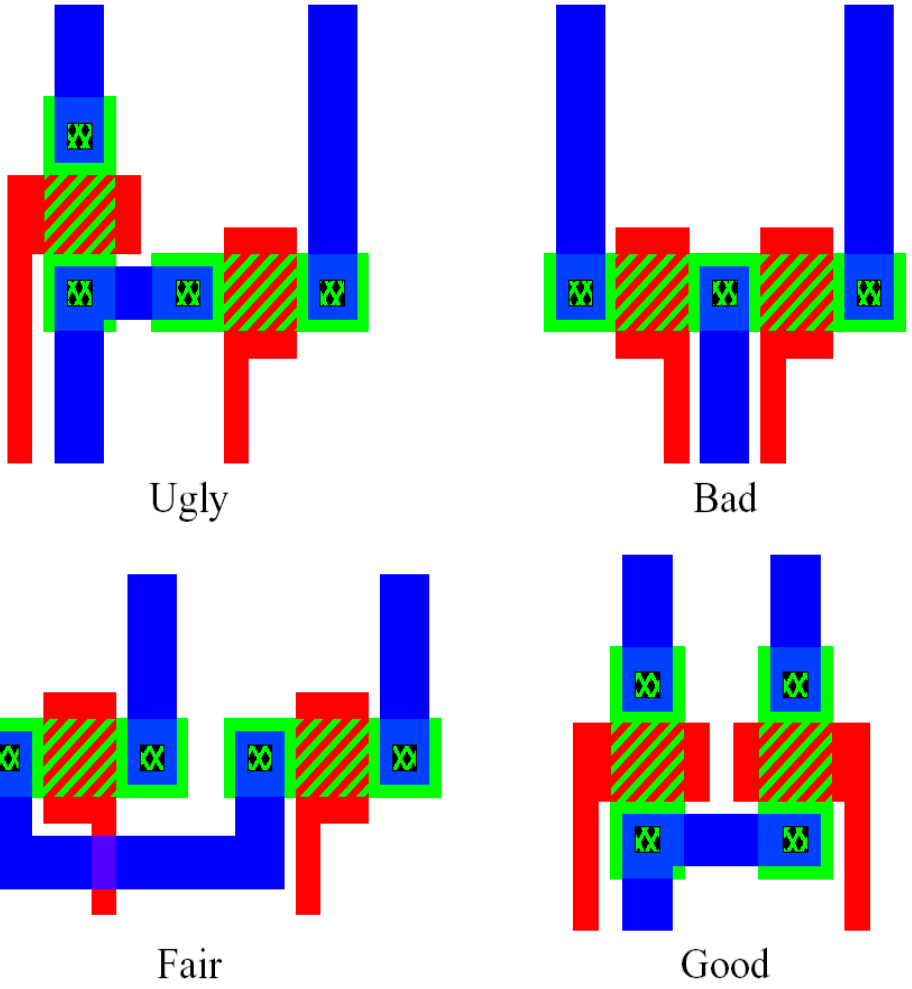




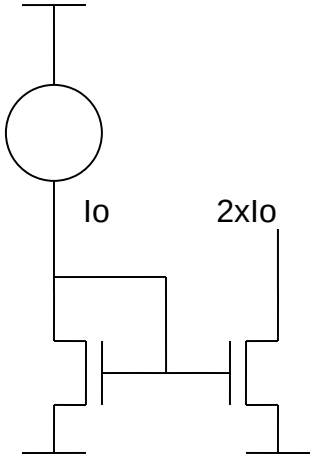
Matching

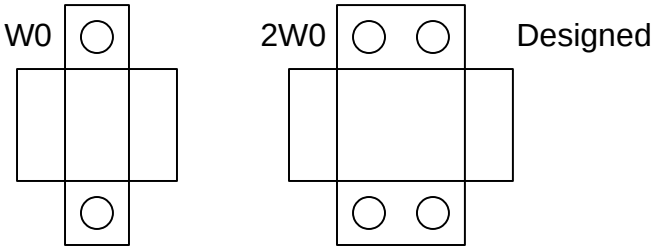
- gleiche Orientierung auf dem Chip

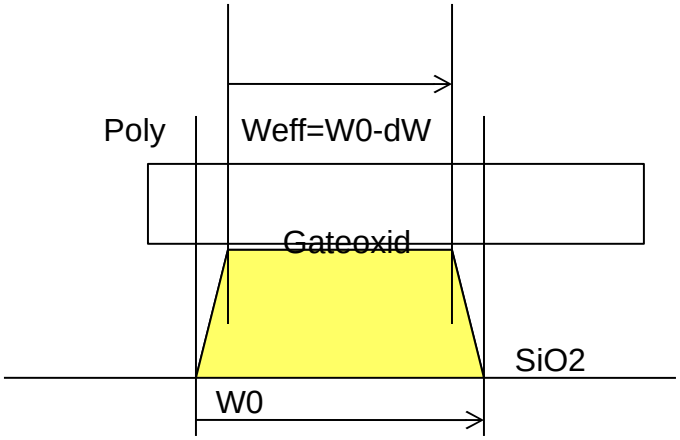
  (Beispiel: Transistorpaar)

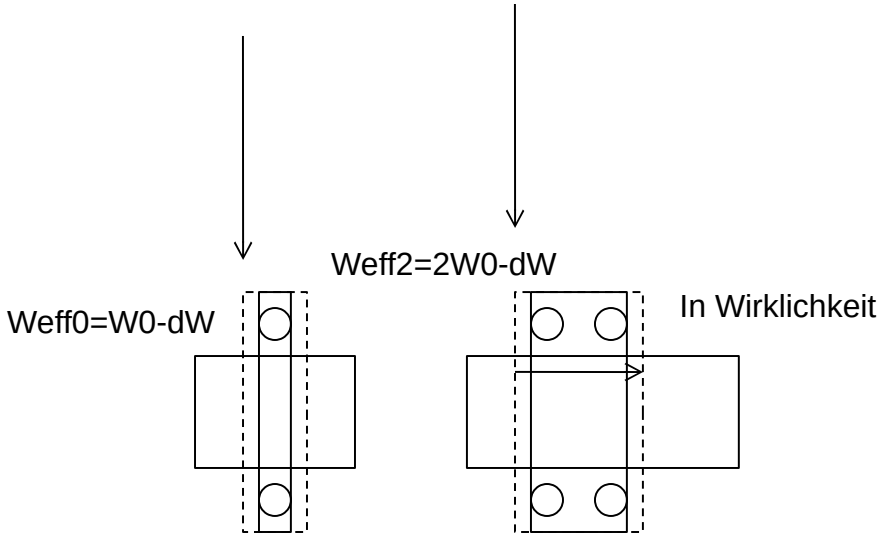


Matching

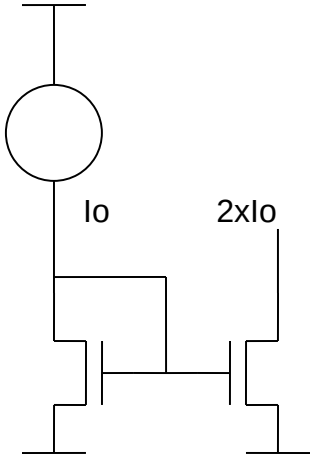

Io
2xIo

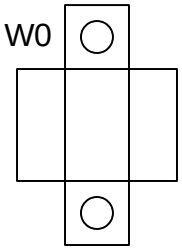

W0
2W0
Designed

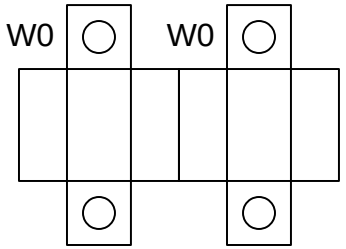

Poly
Weff=W0-dW
Gateoxid
SiO2
W0

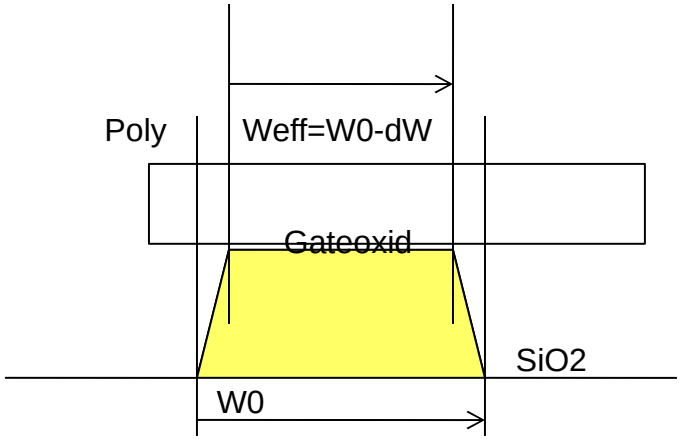

Weff2=2W0-dW
Weff0=W0-dW
In Wirklichkeit
Systematischer Fehler dW
Weff2 != Weff0 * 2

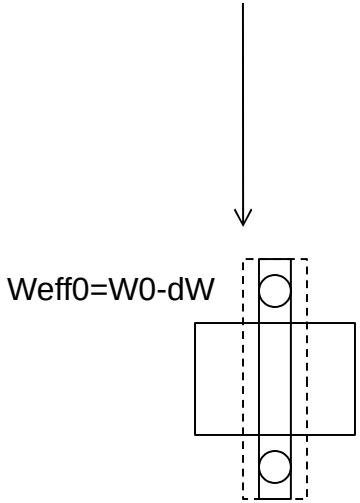
Matching



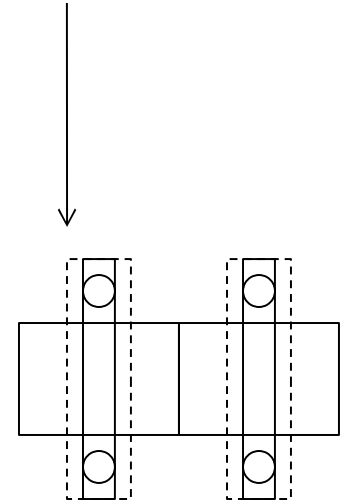






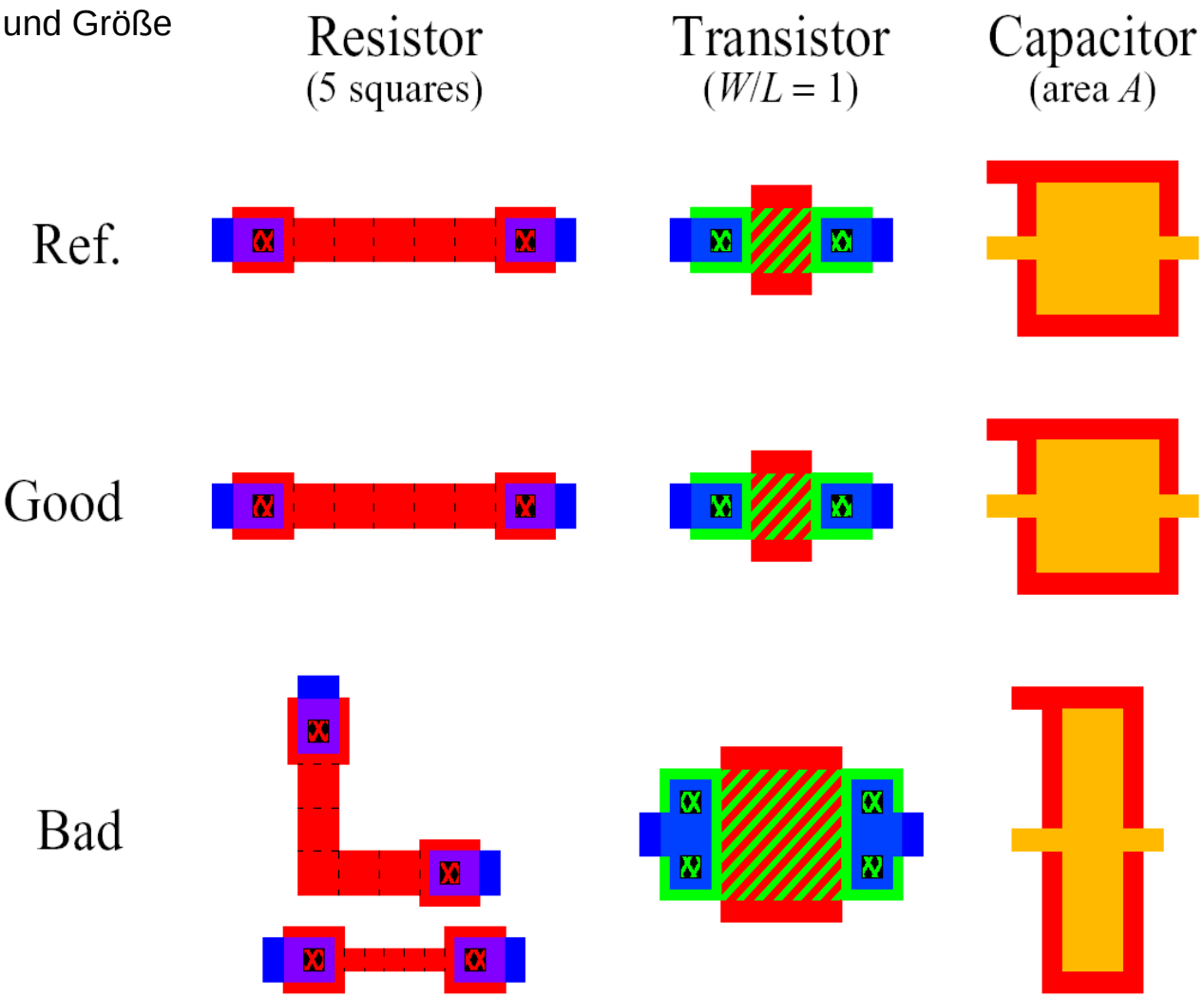


Systematischer Fehler dW



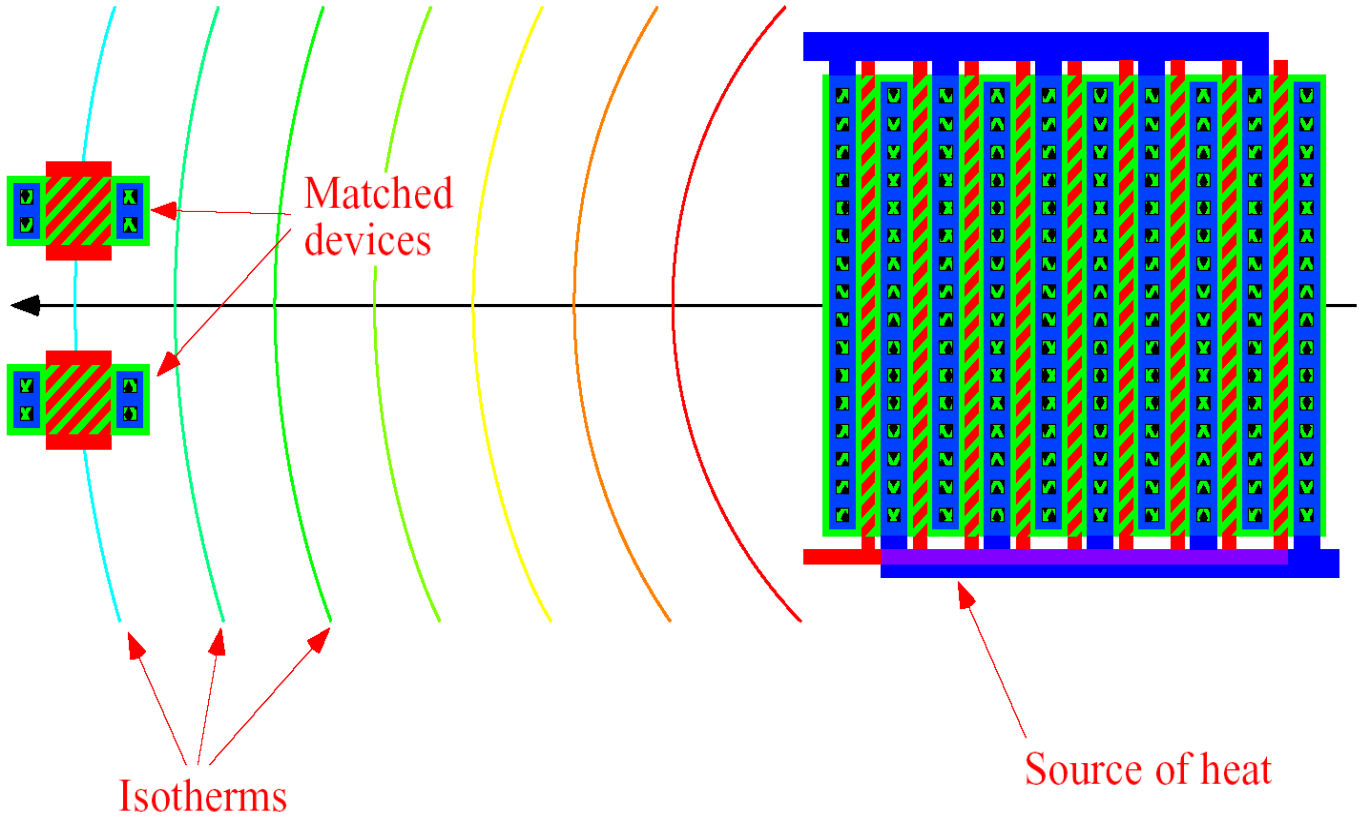
Weff2 = Weff0 * 2

Identische Struktur und Größe

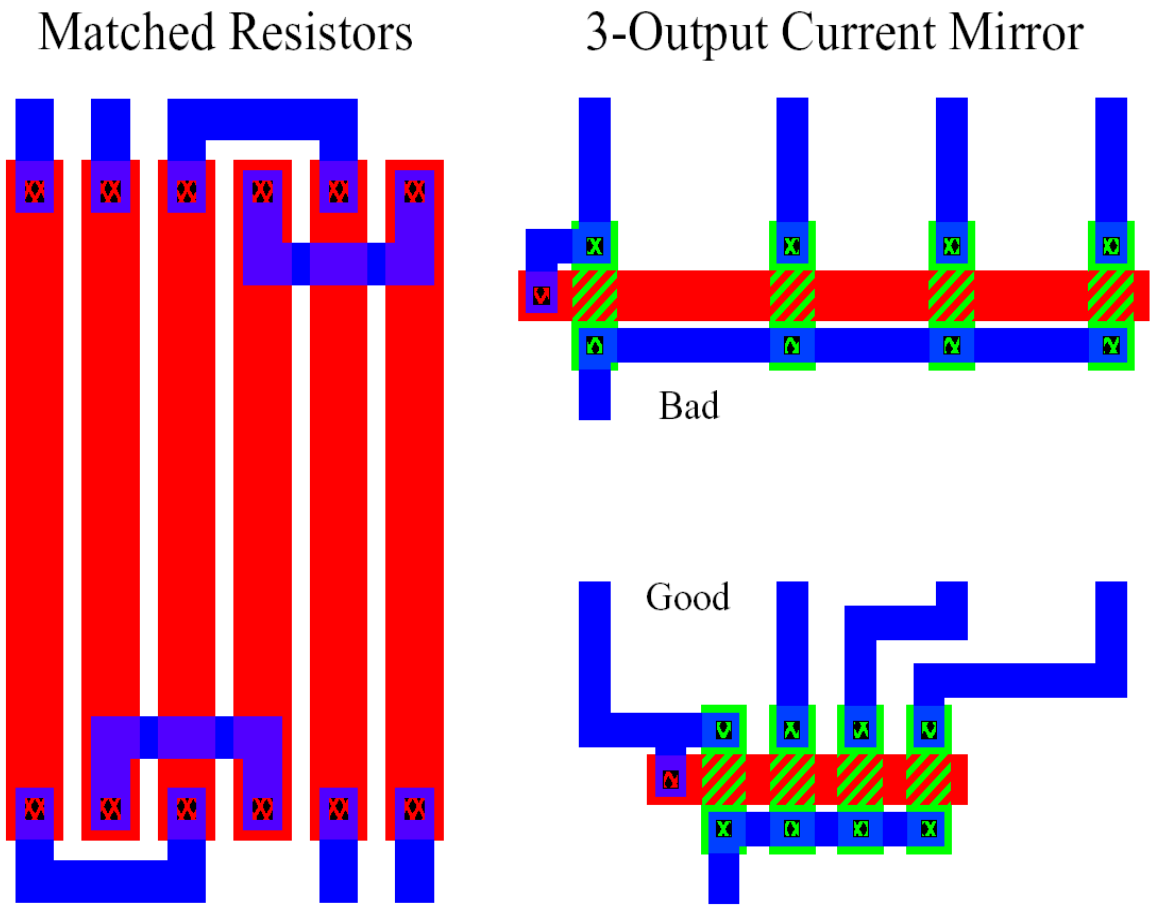


Matching

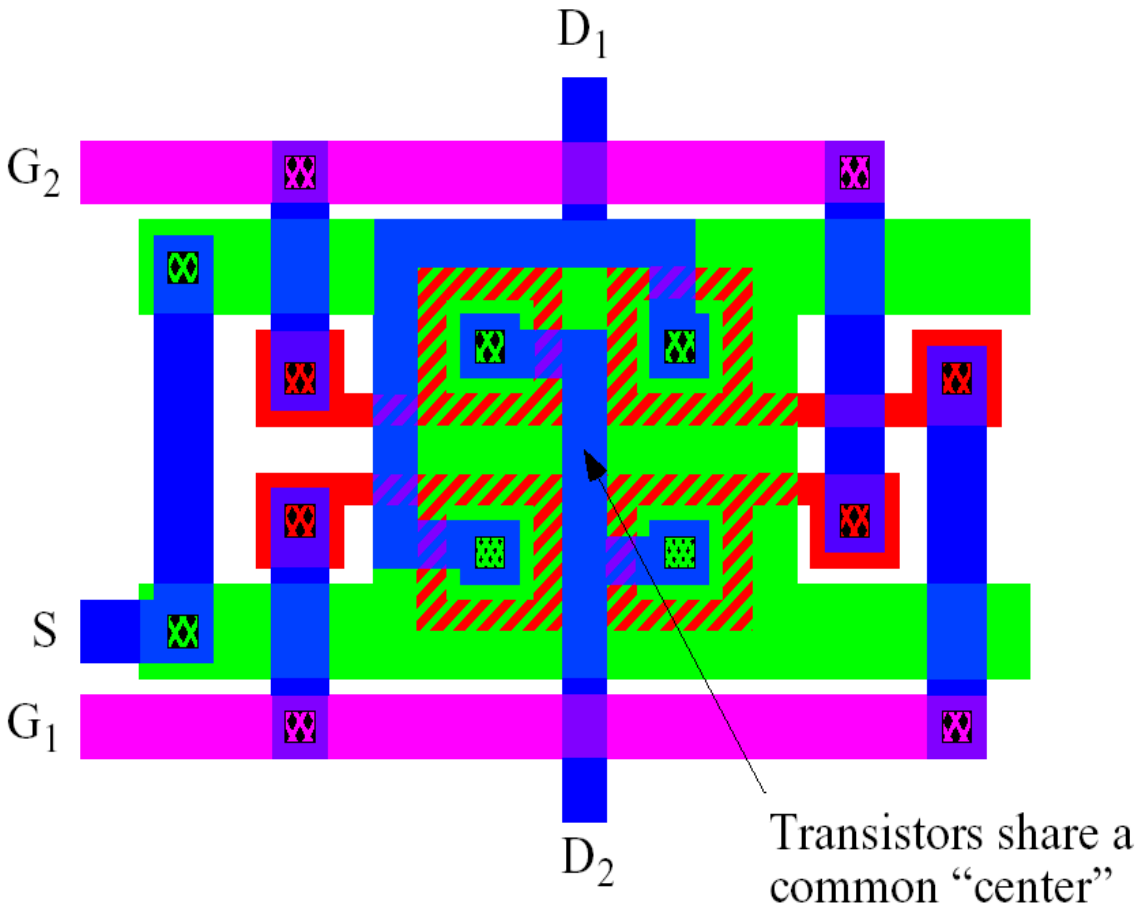
Möglichst gleiche Betriebstemperatur



Minimaler Abstand



Zentrierte Geometrien



Matching

Möglichst identische Umgebung

Stromquellen

Kondensatoren